International Symposium on Low Power Electronics and Design

August 1-3, 2011

Fukuoka Convention Center
Fukuoka, Japan

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Sunday July 31, 2011

18:00	***Reception***

Monday August 1, 2011

AM	***Co-located international workshop on Japanese ultra low power consumption information technology project***	
13:30-14:00	***Welcome by General and Program Co-Chairs (501)*** General chairs: Naehyuck Chang, Seoul National Univ. and Hiroshi Nakamura, Univ. of Tokyo General vice-chair: Koji Inoue, Kyushu Univ. TPC chairs: Kenichi Osada, Hitachi and Massimo Poncino, Politecnico di Torino	
14:00-15:00	**Keynote Talk 1 (501)** Chair: Kenichi Osada, Hitachi	
	Toshihiro Hattori, VP of SoC Business Division, Renesas Mobile Low-power and High-performance Technologies for Mobile SoC in LTE Era	
15:00-15:30	*Break*	
15:30-17:30	**501**	**502-503**
	Session 1.1.1: Low voltage logic and clocking Session Chair: Koichiro Ishibashi, Univ. of Electro-Communications Session Co-Chair: Takahiro Hanyu, Tohoku Univ.	**Session 2.1.1: Low-power design methods and tools** Session Chair: Sri Parameswaran, Univ. of New South Wales Session Co-Chair: Barry Pangrle, Mentor
	Energy Minimum Operation in a Reconfigurable Gate-level Pipelined and Power-Gated Self Synchronous FPGA Benjamin Devlin , Makoto Ikeda, Kunihiro Asada *Univ. of Tokyo*	**FPGA Glitch Power Analysis and Reduction** Warren Wai-Kit Shum, Jason H. Anderson *Univ. of Toronto*
	Variation-aware Clock Network Design Methodology for Ultra-Low Voltage (ULV) Circuits Xin Zhao, Jeremy R. Tolbert, Chang Liu, Saibal Mukhopadhyay, Sung Kyu Lim *Georgia Institute of Technology*	**(B) SAT-based Capture-Power Reduction for At-Speed Broadcast-Scan-Based Test Compression Architectures** *,**Michael A. Kochte , *Kohei Miyase, *Xiaoqing Wen, *Seiji Kajihara, ***Yuta Yamato, *Kazunari Enokimoto, **Hans-Joachim Wunderlich **Kyushu Institute of Technology* ***University of Stuttgart* ****Fukuoka Industry, Science and Technology Foundation*
	Near-/Sub-threshold DLL-based Clock Generator with PVT-Aware Locking Range Compensation Ming-Hung Chang, Chung-Ying Hsieh, Mei-Wei Chen, Wei Hwang *National Chiao Tung Univ.*	**(S) Pulsed-Latch-Based Clock Tree Migration for Dynamic Power Reduction** Hong-Ting Lin, *Yi-Lin Chuang, Tsung-Yi Ho *National Cheng Kung Univ.* **National Taiwan Univ.*
	Investigation of Determinant Factors of Minimum Operating Voltage of Logic Gates in 65-nm CMOS Tadashi Yasufuku, Satoshi Iida, Hiroshi Fuketa, *Koji Hirairi, *Masahiro Nomura, Makoto Takamiya, Takayasu Sakurai *Univ. of Tokyo* **STARC*	**(S) Matched Public PUF: Ultra Low Energy Security Platform** Saro Meguerdichian, Miodrag Potkonjak *UCLA*
		(S) Pinned to the Walls - Impact of Packaging and Application Properties on the Memory and Power Walls Phillip Stanley-Marbell, Victoria Caparrós Cabezas, Ronald Luijten *IBM Research Zurich*
17:30-17:45	*Short Break*	
17:45-19:15	**501**	**502-503**
	Special Session 1: Ultra-Low-Voltage operation Session Chair: Toshinori Sato, Fukuoka Univ. Session Co-Chair: Takanori Hayashida, Fukuoka Univ.	**Embedded Tutorial** Session Chair: Massimo Poncino, Politecnico di Torino
	Takayasu Sakurai, Univ. of Tokyo Designing Ultra-Low Voltage Logic	**Manuj Sabharwal, Intel Corp.** Software power optimization
	Toshiro Hiramoto, Univ. of Tokyo Ultra-Low-Voltage Operation: Device Perspective	
	Mitsumasa Koyanagi, Tohoku Univ. 3D Super Chip Technology to Achieve Low-Power and High-Performance System-on-a Chip	
19:15	***Reception***	

Tuesday August 2, 2011

8:30-9:30	**Keynote Talk 2 (501)** Chair: Naehyuck Chang, Seoul National Univ.
	Kee Sup Kim, Samsung Holistic Low Power Solutions for the New World

9:30-10:00	*Break*	
10:00-12:00	**501**	**502-503**
	Session 1.2.1: Low-power caches Session Chair: Akihiko Inoue, Panasonic Session Co-Chair: Koji Inoue, Kyushu Univ.	**Session 2.2.1: Energy-efficient systems** Session Chair: Kimiyoshi Usami, Shibaura Institute of Technology Session Co-Chair: Tohru Ishihara, Kyushu Univ.
	(B) An Energy-Efficient Adaptive Hybrid Cache Jason Cong, Karthik Gururaj, Hui Huang, Chunyue Liu, Glenn Reinman, Yi Zou *UCLA*	**Versatile High-Fidelity Photovoltaic Module Emulation System** Woojoo Lee, *Younghyun Kim, Yanzhi Wang, *Naehyuck Chang, Massoud Pedram, **Soohee Han *Univ. of Southern California* **Seoul National Univ.* ***Konkuk University*
	Processor Caches with Multi-Level Spin-Transfer Torque RAM Cells Yiran Chen, *Weng-Fai Wong, **Hai Li, ***Cheng-Kok Koh *Univ. of Pittsburgh* **National Univ. of Singapore* ***Polytechnic Institute of New York Univ.* ****Purdue Univ.*	**System Energy Minimization via Joint Optimization of the DC-DC Converter and the Core** Rami A. Abdallah, Pradeep S. Shenoy, Naresh R. Shanbhag, Philip T. Krein *Univ. of Illinois Urbana-Champaign*
	High-Endurance and Performance-Efficient Design of Hybrid Cache Architectures through Adaptive Line Replacement Amin Jadidi, Mohammad Arjomand, Hamid Sarbazi-Azad *Sharif Univ. of Technology & Institute*	**Charge Migration Efficiency Optimization in Hybrid Electrical Energy Storage (HEES) Systems** Yanzhi Wang, *Younghyun Kim, Qing Xie, *Naehyuck Chang, Massoud Pedram *Univ. of Southern California* **Seoul National Univ.*
	TLB Index-based Tagging for Cache Energy Reduction Jongmin Lee, Seokin Hong, Soontae Kim *KAIST*	**Does Low-Power Design Imply Energy Efficiency for Data Centers?** David Meisner, Thomas F. Wenisch *Univ. of Michigan*
12:00-12:30	**501**	**502-503**
	Poster Presentations	
	1.X Posters Session Chair: Vasily Moshnyaga, Fukuoka Univ.	2.X Posters Session Chair: Massimo Poncino, Politecnico di Torino
	Design and Analysis of Metastable-Hardened Flip-Flops in Sub-Threshold Region David Li, Pierce I Jen Chuang, David Nairn, Manoj Sachdev *Univ. of Waterloo*	**Thermal-Aware Bus-Driven Floorplanning** Po-Hsun Wu, Tsung-Yi Ho *National Cheng Kung Univ.*
	12.7-times Energy Efficiency Increase of 16-bit Integer Unit by Power Supply Voltage (VDD) Scaling from 1.2V to 310mV Enabled by Contention-less Flip-Flops (CLFF) and Separated VDD between Flip-Flops and Combinational Logics Hiroshi Fuketa, *Koji Hirairi, Tadashi Yasufuku, Makoto Takamiya, *Masahiro Nomura, *Hirofumi Shinohara, Takayasu Sakurai *Univ. of Tokyo* **STARC*	**An Approach to Energy-Error Tradeoffs in Approximate Ripple Carry Adders** Zvi M. Kedem, *,**Vincent J. Mooney, **,***Kirthi Krishna Muntimadugu **,***Krishna V. Palem New York Univ. *Georgia Institute of Technology **Nanyang Technological Univ. ***Rice Univ.
	8T Single-ended Sub-threshold SRAM with Cross-Point Data-aware Write Operation Yi-Wei Chiu, Jihi-Yu Lin, Ming-Hsien Tu, Shyh-Jye Jou, Ching-Te Chuang *National Chiao Tung Univ.*	**Power and Delay Aware Synthesis of Multi-Operand Adders TargetingLUT-based FPGAs** Taeko Matsunaga, Shinji Kimura, *Yusuke Matsunaga *Waseda Univ.* **Kyushu Univ.*
	Reduction of Minimum Operating Voltage (VDDmin) of CMOS Logic Circuits with Post-Fabrication Automatically Selective Charge Injection Kentaro Honda, Katsuyuki Ikeuchi, *Masahiro Nomura, Makoto Takamiya, Takayasu Sakurai *Univ. of Tokyo* **STARC*	**New Power-aware Placement for Region-based FPGA Architecture Combined with Dynamic Power Gating by PCHM** Ce Li, Yiping Dong, Takahiro Watanabe *Waseda Univ.*
	Eliminating Energy of Same-Content-Cell-Columns of On-Chip SRAM Arrays Bushra Ahsan, Lorena Ndreu, Isidoros Sideris, Yiannakis Sazeides, *Sachin Idgunji, *Emre Özer *Univ. of Cyprus* **ARM*	**Learning to Manage Combined Energy Supply Systems** Azalia Mirhoseini, Farinaz Koushanfar *Rice Univ.*
	A 1.2V 55mW 12bits Self-Calibrated Dual-Residue Analog to Digital Converter in 90 nm CMOS Amir Zjajo, *Jose Pineda de Gyvez *Delft Univ. of Technology* **Eindhoven Univ. of Technology*	**Energy Harvesting by Sweeping Voltage-Escalated Charging of a Reconfigurable Supercapacitor Array** Sehwan Kim, Pai H Chou *Univ. of California, Irvine*
	A Low-Power Direct Digital Frequency Synthesizer Using an Analogue-Sine-Conversion Technique Jun-Hong Weng, Ching-Yuan Yang, Yi-Lin Jhu *National Chung Hsing Univ.*	**On-chip Detection Methodology for Break-Even Time of Power Gated Function Units** Kimiyoshi Usami, Yuya Goto, Kensaku Matsunaga, Satoshi Koyama, *Daisuke Ikebuchi, *Hideharu Amano, **Hiroshi Nakamura *Shibaura Institute of Technology* **Keio Univ.* ***The Univ. of Tokyo*

	A Comparator-Based Cyclic Analog-to-Digital Converter with Boosted Preset Voltage Jong-Kwan Woo, Tae-Hoon Kim, Hyongmin Lee, Sunkwon Kim, Hyunjoong Lee, Suhwan Kim *Seoul National Univ.*	**Improving Energy Efficiency of Multi-Threaded Applications using Heterogeneous CMOS-TFET Multicores** Karthik Swaminathan, Emre Kultursay, Vinay Saripalli, Vijaykrishnan Narayanan, Mahmut Kandemir, Suman Datta *Pennsylvania State Univ.*
		Automated di/dt Stressmark Generation for Microprocessor Power Delivery Networks Youngtaek Kim, Lizy Kurian John *The Univ. of Texas at Austin*
		A Scheduling Algorithm for Consistent Monitoring Results with Solar Powered High-Performance Wireless Embedded Systems Denis Dondi, Piero Zappi, Tajana Šimunic Rosing *Univ. of California San Diego*
		A Design Space Exploration of Transmission-Line Links for On-Chip Interconnect Aaron Carpenter, Jianyun Hu, Michael Huang, Hui Wu, Peng Liu *Univ. of Rochester*
		An Integrated Optimization Framework for Reducing the Energy Consumption of Embedded Real-Time Applications Hideki Takase, Gang Zeng, *Lovic Gauthier, Hirotaka Kawashima, Noritoshi Atsumi, Tomohiro Tatematsu, **Yoshitake Kobayashi, **Shunitsu Kohara, **Takenori Koshiro, *Tohru Ishihara, ***Hiroyuki Tomiyama, Hiroaki Takada *Nagoya Univ.* **Kyushu Univ.* ***Toshiba Corporation* ****Ritsumeikan Univ.*
		Memory Energy Management for an Enterprise Decision Support System Karthik Kumar, *Kshitij Doshi, *Martin Dimitrov, Yung-Hsiang Lu *Purdue Univ.* **Intel Corporation*
12:30-14:00	*Lunch*	
14:00-15:30	**501**	**502-503**
	Session 1.1.2: Low power emerging technology Session Chair: Makoto Takamiya, Univ. of Tokyo Session Co-Chair: Takahiro Hanyu, Tohoku Univ.	**Session 2.1.2: Reliability and thermal issues** Session Chair: Jianfeng Liu, Samsung Session Co-Chair: Youngsoo Shin, KAIST
	(B) Analysis of Power-Performance for Ultra-Thin-Body GeOI Logic Circuits Vita Pi-Ho Hu, Ming-Long Fan, Pin Su, Ching-Te Chuang *National Chiao Tung Univ.*	**TG-based Technique for NBTI Degradation and Leakage Optimization** Chin-Hung Lin, Ing-Chao Lin, Kuan-Hui Li *National Cheng Kung Univ.*
	Delivering on the Promise of Universal Memoryfor Spin-Transfer Torque RAM (STT-RAM) Anurag Nigam, Clinton W Smullen IV, Vidyabhushan Mohan, *Eugene Chen, Sudhanva Gurumurthi, Mircea R Stan *Univ. of Virginia* **Grandis*	**(S) Analysis and Mitigation of NBTI-Induced Performance Degradation for Power-Gated Circuits** Kai-Chiang Wu, Diana Marculescu, *Ming-Chao Lee, *Shih-Chieh Chang *Carnegie Mellon Univ.* **National Tsing Hua Univ.*
	Enhancing Phase Change Memory Lifetime through Fine-Grained Current Regulation and Voltage Upscaling Lei Jiang, Youtao Zhang, Jun Yang *Univ. of Pittsburgh*	**(S) Variation-Aware Static and Dynamic Writability Analysis for Voltage-Scaled Bit-Interleaved 8-T SRAMs** Daeyeon Kim, *Vikas Chandra, *Robert Aitken, David Blaauw, Dennis Sylvester *Univ. of Michigan* **ARM, Inc.*
		(S) Fast Thermal Simulation of 2D/3D Integrated Circuits Exploiting Neural Networks and GPUs Alessandro Vincenzi, Arvind Sridhar, Martino Ruggiero, David Atienza *EPFL*
15:30-16:00	*Break*	
16:00-17:30	**501**	**Lobby**
	Design Contest Session Co-Chair: Chia-Lin Yang, National Taiwan Univ. Session Co-Chair: Yiran Chen, Univ. of Pittsburgh	**Poster Session**
	A Sub-mW All-Digital Signal Component Separator for OFDM Uneven Multi-Level LINC Transmitters Tsan-Wen Chen, Ping-Yuan Tsai, Jui-Yuan Yu, Chen-Yi Lee *National Chiao-Tung Univ.*	**Design and Analysis of Metastable-Hardened Flip-Flops in Sub-Threshold Region** David Li, Pierce I Jen Chuang, David Nairn, Manoj Sachdev *Univ. of Waterloo*
	XRAM: A 4.71Tb/s/W 128×128 Interconnect Fabric for Low Power Signal Processing Sudhir Satpathy, Ronald Dreslinski, Zhiyoong Foo, Dennis Syvester, Trevor Mudge, David Blaauw *Univ. of Michigan*	**12.7-times Energy Efficiency Increase of 16-bit Integer Unit by Power Supply Voltage (VDD) Scaling from 1.2V to 310mV Enabled by Contention-less Flip-Flops (CLFF) and Separated VDD between Flip-Flops and Combinational Logics** Hiroshi Fuketa, *Koji Hirairi, Tadashi Yasufuku, Makoto Takamiya, *Masahiro Nomura, *Hirofumi Shinohara, Takayasu Sakurai *Univ. of Tokyo* **STARC*

A Cloud-Based Energy-Saving Service for Mobile Streaming Applications
Cheng-Kang Hsieh, Chun-Han Lin, Pi-Cheng Hsiu
Research Center for Information Technology Innovation Academia Sinica

8T Single-ended Sub-threshold SRAM with Cross-Point Data-aware Write Operation
Yi-Wei Chiu, Jihi-Yu Lin, Ming-Hsien Tu, Shyh-Jye Jou, Ching-Te Chuang
National Chiao Tung Univ.

Reduction of Minimum Operating Voltage (VDDmin) of CMOS Logic Circuits with Post-Fabrication Automatically Selective Charge Injection
Kentaro Honda, Katsuyuki Ikeuchi, *Masahiro Nomura, Makoto Takamiya, Takayasu Sakurai
Univ. of Tokyo
**STARC*

Eliminating Energy of Same-Content-Cell-Columns of On-Chip SRAM Arrays
Bushra Ahsan, Lorena Ndreu, Isidoros Sideris, Yiannakis Sazeides, *Sachin Idgunji, *Emre Özer
Univ. of Cyprus
**ARM*

A 1.2V 55mW 12bits Self-Calibrated Dual-Residue Analog to Digital Converter in 90 nm CMOS
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**Eindhoven Univ. of Technology*

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Thermal-Aware Bus-Driven Floorplanning
Po-Hsun Wu, Tsung-Yi Ho
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An Approach to Energy-Error Tradeoffs in Approximate Ripple Carry Adders
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,*Krishna V. Palem
New York Univ.
**Georgia Institute of Technology*
***Nanyang Technological Univ.*
****Rice Univ.*

Power and Delay Aware Synthesis of Multi-Operand Adders TargetingLUT-based FPGAs
Taeko Matsunaga, Shinji Kimura, *Yusuke Matsunaga
Waseda Univ.
**Kyushu Univ.*

New Power-aware Placement for Region-based FPGA Architecture Combined with Dynamic Power Gating by PCHM
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Rice Univ.

Energy Harvesting by Sweeping Voltage-Escalated Charging of a Reconfigurable Supercapacitor Array
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On-chip Detection Methodology for Break-Even Time of Power Gated Function Units
Kimiyoshi Usami, Yuya Goto, Kensaku Matsunaga, Satoshi Koyama, *Daisuke Ikebuchi, *Hideharu Amano, **Hiroshi Nakamura
Shibaura Institute of Technology
**Keio Univ.*
***The Univ. of Tokyo*

Improving Energy Efficiency of Multi-Threaded Applications using Heterogeneous CMOS-TFET Multicores
Karthik Swaminathan, Emre Kultursay, Vinay Saripalli, Vijaykrishnan Narayanan, Mahmut Kandemir, Suman Datta
Pennsylvania State Univ.

Automated di/dt Stressmark Generation for Microprocessor Power Delivery Networks
Youngtaek Kim, Lizy Kurian John
The Univ. of Texas at Austin

		A Scheduling Algorithm for Consistent Monitoring Results with Solar Powered High-Performance Wireless Embedded Systems Denis Dondi, Piero Zappi, Tajana Šimunic Rosing *Univ. of California San Diego*
		A Design Space Exploration of Transmission-Line Links for On-Chip Interconnect Aaron Carpenter, Jianyun Hu, Michael Huang, Hui Wu, Peng Liu *Univ. of Rochester*
		An Integrated Optimization Framework for Reducing the Energy Consumption of Embedded Real-Time Applications Hideki Takase, Gang Zeng, *Lovic Gauthier, Hirotaka Kawashima, Noritoshi Atsumi, Tomohiro Tatematsu, **Yoshitake Kobayashi, **Shunitsu Kohara, **Takenori Koshiro, *Tohru Ishihara, ***Hiroyuki Tomiyama, Hiroaki Takada *Nagoya Univ.* **Kyushu Univ.* ***Toshiba Corporation* ****Ritsumeikan Univ.*
		Memory Energy Management for an Enterprise Decision Support System Karthik Kumar, *Kshitij Doshi, *Martin Dimitrov, Yung-Hsiang Lu *Purdue Univ.* **Intel Corporation*
19:00	***Dinner + Cruise***	

Wednesday August 3, 2011		
8:30-9:30	**Keynote Talk 3 (501)** Chair: Massimo Poncino, Politecnico di Torino	
	Sachin Sapatnekar, Univ. of Minnesota The Whys and Hows of Thermal Management	
9:30-10:00	*Break*	
10:00-12:00	**501**	**502-503**
	Session 1.1.3: SRAM Session Chair: Mircea Stan, Univ. of Virginia Session Co-Chair: Kenichi Osada, Hitachi, Ltd.	**Session 2.3.1: Software based techniques for energy optimization** Session Chair: Lovic Gauthier, Kyushu Univ. Session Co-Chair: Vivek Tiwari, Intel Corp.
	A Dynamic body-biased SRAM with Asymmetric Halo Implant MOSFETs Makoto Yabuuchi, Yasumasa Tsukamoto, Hidehiro Fujiwara, Shigeki Tawa, Koji Maekawa, Motoshige Igarashi, Koji Nii *Renesas Electronics Corporation*	**(S) Dynamic Backlight Scaling Optimization for Mobile Streaming Applications** Pi-Cheng Hsiu, Chun-Han Lin, Cheng-Kang Hsieh *Research Center for Information Technology Innovation, Academia Sinica*
	A 1kb 9T Subthreshold SRAM with Bit-Interleaving Scheme in 65nm CMOS Ming-Hung Chang, Yi-Te Chiu, Shu-Lin Lai, Wei Hwang *National Chiao Tung Univ.*	**(S) Object-based Local Dimming for LCD Systems with LED BLUs** Aldhino Anggorosesar, Young-Jin Kim *SunMoon Univ.*
	An Analytical Model for Performance Yield of Nanoscale SRAM Accounting for the Sense Amplifier Strobe Signal Joseph F. Ryan, Sudhanshu Khanna, Benton H. Calhoun *Univ. of Virginia*	**(S) OS-level Power Minimization Under Tight Performance Constraints in General Purpose Systems** Raid Zuhair Ayoub, *Umit Ogras, *Eugene Gorbatov, Yanqin Jin, *Timothy Kam, *Paul Diefenbaugh, Tajana Rosing *Univ. of California at San Diego* **Intel*
	Column-Selection-Enabled 8T SRAM Array with ~1R/1W Multi-Port Operation for DVFS-Enabled Processors Sang Phill Park, Soo Youn Kim, Dongsoo Lee, *Jae-Joon Kim, W. Paul Griffin, Kaushik Roy *Purdue Univ.,* **IBM T.J. Watson Research Center*	**(S) Energy Efficient Scheduling for Multithreaded Programs on General-Purpose Processors** Xin Fan, Shigeru Kusakabe *Kyushu Univ.*
		(S) Software Energy Estimation Based on Statistical Characterization of Intermediate Compilation Code Carlo Brandolese, Simone Corbetta, William Fornaciari *Politecnico di Milano*
		(S) Energy Efficient E-Textile Based Portable Keyboard Mahsan Rofouei, Miodrag Potkonjak, Majid Sarrafzadeh *UCLA*
12:00-13:30	*Lunch*	
13:30-14:30	**Keynote Talk 4 (501)** Chair: Hiroshi Nakamura, Univ. of Tokyo	
	Yasunori Miyahara, Panasonic Next-generation wireless Technologies trends for Ultra Low Energy	
14:30-16:30	**501**	**502-503**
	Session 1.3.1: Innovations in low-power analog Session Chair: Amir Zjajo, Delft Univ. of Technology Session Co-Chair: Suhwan Kim, Seoul National Univ.	**Special Session 2: Green HPC** Session Chair: Takeshi Nanri, Kyushu Univ. Session Co-Chair: Toshinori Sato, Fukuoka Univ.

	(B) A Low-Power Referenceless Clock and Data Recovery Circuit with Clock-Edge Modulation for Biomedical Sensor Applications Sunkwon Kim, Jong-Kwan Woo, Woo-Yeol Shin, Gi-Moon Hong, Hyongmin Lee, Hyunjoong Lee, Suhwan Kim *Seoul National Univ.*	**Satoshi Matsuoka, Tokyo Institute of Technology** Making TSUBAME2.0, the World's Greenest Production Supercomputer, Even Greener
	A 92.4dB SNDR 24kHz DeltaSum Modulator Consuming 352 muW Liyuan Liu, Dongmei Li, Yafei Ye, Zhihua Wang *Tsinghua Univ.*	**Ken Takeuchi, Univ. of Tokyo** Green High Performance Storage Class Memory & NAND Flash Memory Hybrid SSD System
	A CMOS Readout Integrated Circuit with Wide Dynamic Range for a CNT Bio-Sensor Array System Hyunjoong Lee, Hyongmin Lee, Jong-Kwan Woo, Sunkwon Kim, Young June Park, Suhwan Kim *Seoul National Univ.*	**Mitsuo Yokokawa, RIKEN** The K Computer
	Experimental Investigation of Inductorless, Single-Stage Boost Rectification for sub-mW Electromagnetic Energy Harvesters Gyorgy D. Szarka, Plamen P. Proynov, Bernard H. Stark, Stephen G. Burrow, Neville McNeill *Univ. of Bristol*	
16:30-17:00	*Break*	
17:00-18:30	**501**	**502-503**
	Session 1.2.2: Low power micro-architecture Session Chair: Takashi Miyamori, Toshiba Session Co-Chair: Vasily Moshnyaga, Fukuoka Univ.	**Session 2.2.2: Power issues in interconnect and domain-specific architecture** Session Chair: Farhad Mehdipour, Kyushu Univ. Session Co-Chair: Naehyuck Chang, Seoul National Univ.
	A 98 GMACs/W 32-Core Vector Processor in 65nm CMOS Xun He, Dajiang Zhou, Xin Jin, Satoshi Goto *Waseda Univ.*	**(B) Analysis and Mitigation of Lateral Thermal Blockage Effect of Through-Silicon-Via in 3D IC Designs** Yibo Chen, *Eren Kursun, *Dave Motschman, *Charles Johnson, Yuan Xie *Penn State Univ.* **IBM*
	(S) Thread Shuffling: Combining DVFS and Thread Migration toReduce Energy Consumptions for Multi-core Systems Qiong Cai, Jose Gonzalez, Grigorios Magklis, Pedro Chaparro, Antonio Gonzalez *Intel*	**NoC Frequency Scaling with Flexible-Pipeline Routers** Pingqiang Zhou, Jieming Yin, Antonia Zhai, Sachin S Sapatnekar *Univ. of Minnesota*
	(S) Fast and Energy-Efficient Constant-Coefficient FIR Filters Using Residue Number System Piotr Patronik, Krzysztof Berezowski, *Stanislaw J. Piestrak, Janusz Biernat, **Aviral Shrivastava *Wroclaw Univ. of Technology* **IRISA, 6 rue de Kerapont* ***Arizona State Univ.*	**IMPACT: IMPrecise Adders for Low-power Approximate CompuTing** Vaibhav Gupta, Debabrata Mohapatra, Sang Phill Park, Anand Raghunathan, Kaushik Roy *Purdue Univ.*
	(S) A Fast, Accurate and Simple Critical Path Monitor for Improving Energy-Delay Product in DVS Systems Junyoung Park, Jacob A. Abraham *The Univ. of Texas at Austin*	
18:30	***Closing Remarks***	