Conference Program

Sheraton La Jolla Hotel,
La Jolla, California, USA

Message from the General Chairs

On behalf of the Organizing Committee, it is our pleasure to welcome you to the 2014 ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED 2014), which is held in La Jolla, California, on August 11-13, 2014. La Jolla in Spanish means "The Jewel". It is the Jewel of America's finest city, San Diego. La Jolla is located 15 minutes from downtown San Diego. It features shimmering ocean views to timeless landmarks. It is home to renowned institutions, such as the Scripps Institution of Oceanography, the Stephen Birch Aquarium & Museum, and the University of California, San Diego.

ISLPED (www.islped.org) is the premier forum for presentation of recent advances in all aspects of low-power design and technologies, ranging from process and circuit technologies, simulation and synthesis tools, to system-level design and software optimization. This year we have kept up the tradition of having outstanding contributions from the low-power design community. The Technical Program Chairs, Muhammad Khellah (Intel) and Renu Mehra (Synopsys), have worked hard to put together an excellent Technical Program. Many thanks go to the Technical Program Committee comprising of leading researchers in the area of low-power design and to Professors Mingoo Seok and Yiran Chen, for chairing the Low-Power Design Contest.

The ISLPED 2014 Organizing Committee has been working tirelessly to bring you a world-class conference experience: Xiangyu Dong and Jack Sampson, Local Arrangements Chairs; Eren Kursun, Industrial Liaison; Yu Wang, Treasurer and Registration Chair; Theo Theocharides, Web Chair; and Deming Chen, Baris Taskin, Jose Ayala, Publicity Chairs. We are also grateful to the Executive Committee, chaired by Massoud Pedram, for their continued guidance in making ISLPED 2014 a great success.

ISLPED 2014 has been fortunate to receive strong support from the industry. In particular, we appreciate the generous financial support from Intel, Synopsys, Qualcomm, IBM, Huawei, and Microsoft for ISLPED 2014. ISLPED 2014 is sponsored by ACM, ACM-SIGDA, IEEE, and IEEE-CAS, with technical support from the SSCS and EDS. We hope that you will enjoy the excellent ISLPED 2014 program this year, and have a pleasant, enriching and memorable experience at La Jolla.

Tanay Karnik, Intel
ISLPED '14 General Co-Chair

Yuan Xie, UCSB
ISLPED '14, General Co-Chair

Message from the Program Chairs

It is our great pleasure to welcome you to the *2014 ACM/IEEE International Symposium on Low Power Electronics and Design – ISLPED'14,* in the beautiful city of La Jolla, CA, USA. The mission of our symposium is to provide education and technical enrichment for professionals and promote advancement of the state-of-the-art in the area of low power electronics and design.

This year, the call for papers attracted 184 submissions from Asia, Africa, Europe, and North & South America. The Technical Program Committee (TPC) accepted a total of 63 papers with 43 full-length presentations and 20 posters. The accepted papers cover a variety of low-power topics in technologies, circuits, logic & architecture, CAD Tools & methodologies, systems & platforms, and software and applications. We are very thankful to the authors for their contributions and to our TPC members for volunteering their valuable time and effort in reviewing the papers, and providing feedback to the authors. In addition to the above accepted papers, this year's program features:

- Three Keynote Speeches by Dr. Karim Arabi, Qualcomm; Prof. Jason Cong, UCLA, and Dr. Partha Ranganathan, Google
- Industry Focus Session on Low-power Circuits & Technologies
- Four Embedded Invited Papers on Emerging Low-power Topics
- Embedded Tutorial by industry EDA experts

We hope the above talks will complement our main program by providing you with an in-depth understanding of the low-power state-of-the-art as well as gives you valuable insights into future trends.

Finally, we hope that you will find the overall program interesting and thought-provoking and that the symposium will provide you with a valuable opportunity to share ideas with other researchers and practitioners from institutions around the world.

Renu Mehra, Synopsys
ISLPED '14 Program Co-Chair

Muhammad M. Khellah, Intel
ISLPED '14 Program Co-Chair

Program at a Glance: Monday

8:30-8:45	Welcome Address: University Room	
8:45-9:45	Keynote 1: University Room	
	Low power Design Techniques In Mobile Processors *Karim Arabi, Qualcomm*	
10:15-11:55	Session 1A: University Room	Session 1B: Executive Room
	Photonics, Spintronics, Approximate Computing and Front-End Throttling	Approximate Computing and Quality Driven Power-Aware System Design
11:55-1:30	Posters: Coast Ballroom	
	Lunch: Coast Ballroom	
1:30-2:45	Session 2A: University Room	Session 2B: Executive Room
	Emerging Technologies	Energy-Efficient Systems Using Emerging Non-volatile Memory Technologies
2:45-3:15	Break	
3:15-4:30	Session 3A: University Room	Session 3B: Executive Room
	Clock and IO Circuit Techniques	Thermal-Aware Design: from Device to System
4:30-4:45	Break	
4:45-6:00	Session 4A: University Room	Session 4B: Executive Room
	Industry Special Session	Embedded Tutorial
6:00 - 8:00	Industry reception: Coast Ballroom	

Program at a Glance: Tuesday

8:45-9:45	Keynote 2: University Room	
	Accelerator-Rich Architectures – from Single-chip to Datacenters, *Jason Cong, UCLA*	
9:30-10:00	Break	
10:00-11:40	Session 5A: University Room	Session 5B: Executive Room
	GPU Voltage Noise, Uncore Power Modeling, Memory Power Management, and Testing	CAD for Low Power and Reliability
11:40-12:20	Posters: Coast Ballroom	
12:20-1:30	Lunch: Coast Ballroom	
1:30-2:45	Session 6A: University Room	Session 6B: Executive Room
	Energy Efficient Digital Circuit Techniques	Optimizing Computation and Communication in Mobile Systems
2:45-3:15	Break	
3:15-4:30	Session 7A: University Room	Session 7B: Executive Room
	Voltage Reference and Power Converter Circuits	Variation and Reliability Consideration for Low-Power Systems
4:30-4:45	Break	
4:45-6:00	Session 8A: University Room	Session 8B: Executive Room
	Design Contest	Poster Presentations
6:00 - 9:00	Dinner + Banquet: Birch Aquarium	

Program at a Glance: Wednesday

8:30 - 9:30	Keynote 3: University Room	
	The New (System) Balance of Power and Opportunities for Optimizations, *Partha Ranganathan, Google*	
9:30-10:00	Break	
10:00-11:40	Session 9A: University Room	Session 9B: Executive Room
	Energy Efficient Cache and Memory Design	Energy Harvesting and Energy-Aware System Design
11:40-12:00	Break	

ISLPED 2014 Program: Monday

8:30-8:45	**Welcome Address: University Room**	
8:45-9:45	**Keynote 1: University Room**	
	Low power Design Techniques In Mobile Processors Karim Arabi, VP of Engineering for Qualcomm Research *Session Chair: Yuan Xie (University of California, Santa Barbara)*	
10:15-11:55	**Session 1A: University Room**	**Session 1B: Executive Room**
	Photonics, Spintronics, Approximate Computing and Front-End Throttling *Session Chairs: Hans Jacobson (IBM) and Umit Ogras (Arizona State University)*	**Approximate Computing and Quality Driven Power-Aware System Design** *Session Chairs: Xiangyu Dong (Qualcomm) and Vivek Joy (Intel)*
10:15-10:40	**EcoLaser: An Adaptive Laser Control for Energy Efficient On-Chip Photonic Interconnects** Yigit Demir, Nikos Hardavellas *Northwestern University*	***(Best Paper Nominee)*** **AxNN: Energy Efficient Neuromorphic Systems using Approximate Computing** Swagath Venkataramani; Ashish Ranjan; Kaushik Roy; Anand Raghunathan *Purdue University*
10:40-11:05	**A Model for Array-based Approximate Arithmetic Computing with Application to Multiplier and Squarer Design** Botang Shao, Peng Li *Texas A&M University*	**TONE: Adaptive Temperature Optimization for the Next Generation Video Encoders** Daniel Palomino[1]; Muhammad Shafique[2]; Altamiro Susin[1]; Joerg Henkel [2] *[1]Federal University of Rio Grande do Sul; [2]Karlsruhe Institute of Technology*

ISLPED 2014 Program: Monday

11:05-11:30	**SPINDLE: SPIntronic Deep Learning Engine for Large-scale Neuromorphic Computing** Shankar Ganesh Ramasubramanian; Rangharajan Venkatesan; Mrigank Sharad; Kaushik Roy; Anand Raghunathan *Purdue University*	**StoRM: Stochastic Recognition and Mining Processor** Vinay Chippa; Swagath Venkataramani; Kaushik Roy; Anand Raghunathan *Purdue University*
11:30-11:55	**Adaptive Front-End Throttling for Superscalar Processors** Wei Zhang; Hang Zhang; John Lach *University of Virginia*	**Approximate Compressed Sensing: Ultra-Low Power Biosignal Processing via Aggressive Voltage Scaling on a Hybrid Memory Multi-core Processor** Daniele Bortolotti[1]; Hossein Mamaghanian[2]; Andrea Bartolini[1]; Maryam Ashouei[3]; Jan Stuijt[3]; Pierre Vandergheynst[2]; Luca Benini[1]; David Atienza[2] *[1]University of Bologna; [2]École polytechnique fédérale de Lausanne; [3]IMEC / Holst Center*
11:55-1:30	**Posters: Coast Ballroom**	
	Lunch: Coast Ballroom	

ISLPED 2014 Program: Monday

	Session 2A: University Room	Session 2B: Executive Room
1:30-2:45	**Emerging Technologies** *Session Chairs: Arijit Raychowdhury (Georgia Institute of Technology) and Patrick Mercier (University of California, San Diego)*	**Energy-Efficient Systems Using Emerging Non-Volatile Memory Technologies** *Session Chairs: Vijay Raghunathan (Purdue University) and Zhenyu Sun (Broadcom)*
1:30-1:55	***(Best Paper)*** **An On-chip Autonomous Thermoelectric Energy Management System for Energy-Efficient Active Cooling** Borislav Alexandrov; Khondker Z. Ahmed; Saibal Mukhopadhyay *Georgia Institute of Technology*	**Making B+-Tree Efficient in PCM-Based Main Memory** Ping Chi; Wang-Chien Lee; Yuan Xie *Pennsylvania State University*
1:55-2:20	**Tunnel FET-Based Ultra-Low Power, Low-Noise Amplifier Design for Bio-signal Acquisition** Huichu Liu[1]; Mahsa Shoaran[2]; Xueqing Li[1]; Suman Datta[1]; Alexandre Schmid[2]; Vijaykrishnan Narayanan[1] *[1]Pennsylvania State University; [2]Swiss Federal Institute of Technology (EPFL);*	**Sleep-Aware Variable Partitioning for Energy-Efficient Hybrid PRAM and DRAM Main Memory** Chenchen Fu[1]; Mengying Zhao[1]; Chun Jason Xue[1]; Alex Orailoglu[2] *[1]City University of Hong Kong; [2]University of California*
2:20-245	***(Invited paper)*** **Performance Modeling for Emerging Interconnect Technologies in CMOS and Beyond-CMOS Circuits** Sou-Chi Chang, Rouhollah M. Iraei, Vachan Kumar, Ahmet Ceyhan, and Azad Naeemi *Georgia Tech University.*	**DR. Swap: Energy-Efficient Paging for Smartphones** Kan Zhong[1]; Xiao Zhu[1]; Tianzheng Wang[2]; Dan Zhang[1]; Xianlu Luo[1]; Duo Liu[1]; Weichen Liu[1]; Edwin Sha[1] *[1]Chongqing University; [2]University of Toronto*
2:45-3:15	**Break**	

ISLPED 2014 Program: Monday

	Session 3A: University Room	Session 3B: Executive Room
3:15-4:30	**Clock and IO Circuit Techniques** *Session Chairs: Gordon Gammie (MediaTek) and Jie Gu (Maxlinear)*	**Thermal-Aware Design: from Device to System** *Session Chairs: Jiang Hu (Texas A&M University) and Umit Ogras (Arizona State University)*
3:15-3:40	**Quasi-Resonant Clocking: A Run-time Control Approach for True Voltage-Frequency-Scalability** Visvesh Sathe *University of Washington*	**Dynamic Thermal Management for FinFET-Based Circuits Exploiting the Temperature Effect Inversion Phenomenon** Woojoo Lee; Yanzhi Wang; Tiansong Cui; Shahin Nazarian; Massoud Pedram *University of Southern California*
3:40-4:05	**An Energy-efficient 2.5D Through-silicon Interposer I/O with Self-adaptive Adjustment of Output-voltage Swing** Dongjun Xu[1]; Sai Manoj P D[1]; Hantao Huang[1]; Ningmei Yu[2]; Hao Yu[1] *[1]Nanyang Technological University; [2]Xian University of Technology;*	**Buffered Clock Tree Synthesis Considering Self-Heating Effects** Chung-Wei Lin[1]; Tzu-Hsuan Hsu[2]; Xin-Wei Shih[2]; Yao-Wen Chang[2] *[1]University of California, Berkeley; [2]National Taiwan University*
4:05-4:30	**Reconfigurable Regenerator-based Interconnect Design for Ultra-Dynamic-Voltage-Scaling Systems** Seongjong Kim; Mingoo Seok *Columbia University*	**Therminator: A Thermal Simulator for Smartphones Producing Accurate Chip and Skin Temperature Maps** Qing Xie; Mohammad Javad Dousti; Massoud Pedram *University of Southern California*
4:30-4:45	**Break**	

ISLPED 2014 Program: Monday

	Session 4A: University Room	Session 4B: Executive Room
4:45-6:00	**Industry Special Session** *Session Chair: Muhammad Khellah (Intel)*	**Embedded Tutorial** *Session Chairs: Massimo Poncino (Politecnico di Torino) and Renu Mehra (Synopsys)*
4:45-5:10	***(Invited Paper)*** **Challenges in Low-Power Analog Integrated Circuit Design for Sub-28nm CMOS Technologies** Amr Fahim *Semtech Corp.*	***(Embedded Tutorial)*** **Failing to Fail - Achieving Success in Advanced Low Power Design using UPF** Rick Koster[1], Shreedhar Ramachandra[2], Sushma Honnavara Prasad[3] *[1]Mentor Graphics; [2]Synopsys Inc.; [3]Broadcom Corp*
5:10-5:35	***(Invited paper)*** **Process and design solutions for exploiting FD-SOI technology towards energy efficient SOCs** Philippe Flatresse *ST Microelectronics*	
5:35-6:00	***(Invited paper)*** **Embedded STT-MRAM for Emerging Mobile Applications: Toward Unified eNVM Solution** Kangho Lee, Seung H. Kang *Qualcomm*	
6:00 - 8:00	**Industry reception: Coast Ballroom**	

ISLPED 2014 Program: Tuesday

8:45-9:45	**Keynote 2: University Room** **Accelerator-Rich Architectures – from Single-Chip to Datacenters** Jason Cong, University of California, Los Angeles *Session Chair: Tanay Karnik (Intel)*	
9:30-10:00	**Break**	
	Session 5A: University Room	**Session 5B: Executive Room**
10:00-11:40	**GPU Voltage Noise, Uncore Power Modeling, Memory Power Management, and Testing** *Session Chairs: John Sampson (Penn State University) and Yaojun Zhang (Qualcomm)*	**CAD for Low Power and Reliability** *Session Chairs: Zhiru Zhang (Cornell University) and Yiran Chen (University of Pittsburgh)*
10:00-10:25	***(Best Paper Nominee)*** **GPUVolt: Modeling and Characterizing Voltage Noise in GPU Architectures** Jingwen Leng[1], Yazhou Zu[1], Minsoo Rhu[1], Meeta Sharma Gupta[2] and Vijay Janapa Reddi[1] *[1]The University of Texas at Austin; [2]IBM T.J. Watson*	**Algorithms for Power-Efficient QoS in Application-Specific NoCs** Hao He, Gongming Yang and Jiang Hu *Texas A&M University*
10:25-10:50	**Empirically Derived Abstractions in Uncore Power Modeling for a Server-Class Processor Chip** Hans Jacobson, Arun Joseph, Dharmesh Parikh, Pradip Bose and Alper Buyuktosunoglu *IBM*	**Design and CAD Methodologies for Low Power Gate-level Monolithic 3D ICs** Shreepad Panth[1], Kambiz Samadi[2], Yang Du[2] and Sung Kyu Lim[1] *[1]Georgia Institute of Technology; [2]Qualcomm Research*

ISLPED 2014 Program: Tuesday

10:50-11:15	**Content-Driven Memory Pressure Balancing and Video Memory Power Management for Parallel High Efficiency Video Coding** Felipe Sampaio[1], Muhammad Shafique[2], Bruno Zatt[1], Sergio Bampi[1] and Joerg Henkel[2] *[1]Federal University of Rio Grande do Sul; [2]Karlsruhe Institute of Technology*	**Efficient NBTI Modeling Technique Considering Recovery Effects** Reef Eilers[1], Malte Metzdorf[1], Domenik Helms[1] and Wolfgang Nebel[1,2] *[1]OFFIS Institute for Computer Science; [2]University of Oldenburg*
11:15-11:40	**Software Canaries: Software-based Path Delay Fault Testing for Variation-aware Energy-efficient Design** John Sartori[1] and Rakesh Kumar[2] *[1]University of Minnesota; [2]University of Illinois at Urbana-Champaign*	***(Invited Paper)*** **Bridging High Performance and Low Power in the era of Heterogeneous Computing** Ruchir Puri *IBM*
11:40-12:20	**Posters: Coast Ballroom**	
12:20-1:30	**Lunch: Coast Ballroom**	

ISLPED 2014 Program: Tuesday

	Session 6A: University Room	Session 6B: Executive Room
1:30-2:45	**Energy Efficient Digital Circuit Techniques** *Session Chairs: Rob Gilmore (Qualcomm) and Joyce Kwong (TI)*	**Optimizing Computation and Communication in Mobile Systems** *Session Chairs: Sujit Dey (University of California, San Diego) and Yiran Chen (University of Pittsburgh)*
1:30-1:55	**CASA: Correlation-Aware Speculative Adders** Gai Liu; Ye Tao; Mingxing Tan; Zhiru Zhang *Cornell University*	**A case for leveraging 802.11p for Direct Phone-to-Phone Communications** Pilsoon Choi[1]; Jason Gao[1]; Nadesh Ramanathan[2]; Mengda Mao[2]; Shipeng Xu[2]; Chirn-Chye Boon[2]; Suhaib Fahmy[2]; Li-Shiuan Peh[1] *[1]MIT; [2]NTU;*
1:55-2:20	**Synergistic Circuit and System Design for Energy-Efficient and Robust Domain Wall Caches** Seyedhamidreza Motaman; Anirudh Iyengar; Swaroop Ghosh *University of South Florida*	***(Invited Paper)*** **Leakage Mitigation Techniques in Smartphone SoCs"** John Redmond *Broadcom Corporation*
2:20-2:45	**Timing Errors in LDPC Decoding Computations with Overscaled Supply Voltage** Behnam Sedighi[1]; N. Prasanth Anthapadmanabhan[2]; Dusan Suvakovic[2] *[1]University of Notre Dame; [2]Bell Labs, Alcatel-Lucent;*	
2:45-3:15	**Break**	

ISLPED 2014 Program: Tuesday

	Session 7A: University Room	Session 7B: Executive Room
3:15-4:30	**Voltage Reference and Power Converter Circuits** *Session Chairs: Swaroop Ghosh (University of Florida) and Nilanjan Banerjee (Qualcomm)*	**Variation and Reliability Consideration for Low-Power Systems** *Session Chairs: Eli Bozorgzadeh (University of California, Irvine) and Younghyun Kim (Purdue University)*
3:15-3:40	**2.3 ppm/°C, 40 nW MOSFET-Only Voltage Reference** Oscar Elisio Mattia; Hamilton Klimach; Sergio Bampi *Federal University of Rio Grande do Sul*	**Aging Mitigation of Power Supply-Connected Batteries** Jaemin Kim[1]; Alma Proebstl[2]; Samarjit Chakraborty[2]; Naehyuck Chang[1] *[1]Seoul National University; [2]TU Munich*
3:40-4:05	**A Bipolar ±40 mV Self-Starting Boost Converter with Transformer Reuse for Thermoelectric Energy Harvesting** Nachiket Desai; Yogesh Ramadass; Anantha Chandrakasan *Massachusetts Institute of Technology*	**Variation tolerant design of a vector processor for Recognition, Mining and Systhesis** Vivek Kozhikkottu[1]; Swagath Venkataramani[1]; Sujit Dey[2]; Anand Raghunathan[1] *[1]Purdue University; [2]University of California, San Diego*
4:05-4:30	**Impact of Process Variation in Inductive Integrated Voltage Regulator on Delay and Power of Digital Circuits** Monodeep Kar[1]; Harish Krishnamurthy[2]; Sergio Carlo[1]; Saibal Mukhopadhyay[1] *[1]Georgia Institute of Technology;[2]Intel*	**Thermal-Aware Layout Planning for Heterogeneous Datacenters** Reza Azimi; Xin Zhan; Sherief Reda *Brown University*
4:30-4:45	**Break**	
4:45-6:00	**Session 8A: University Room** **Design Contest**	**Session 8B: Executive Room** **Poster Presentations**
6:00 -	**Dinner + Banquet: Birch Aquarium**	

ISLPED 2014 Program: Wednesday

8:30-9:30	**Keynote 3: University Room**	
	The New (System) Balance of Power and Opportunities for optimizations Dr. Partha Ranganathan, Google *Session Chairs: Muhammad Khellah (Intel) and Renu Mehra (Synopsys)*	
9:30-10:00	**Break**	
10:00-11:40	**Session 9A: University Room**	**Session 9B: Executive Room**
	Energy Efficient Cache and Memory Design *Session Chairs: Xi Chen (Qualcomm) and Zhenyu Sun (Broadcom)*	**Energy Harvesting and Energy-Aware System Design** *Session Chairs: Naehyuck Chang (Seoul National University) and Hyung Gyu Lee (Daegu University)*
10:00-10:25	**eDRAM-Based Tiered-Reliability Memory with Applications to Low-Power Frame Buffers** Kyungsang Cho[1,2]; Yongjun Lee[1,2]; Younghwan Oh[2]; Gyoo-cheol Hwang[1]; Jae W. Lee[2] *[1]Samsung Electronics; [2]Sungkyunkwan University*	***(Best Paper)*** **Fast Photovoltaic Array Reconfiguration for Partial Solar Powered Vehicles** Jaemin Kim[1]; Yanzhi Wang[2]; Massoud Pedram[2]; Naehyuck Chang[1] *[1]Seoul National University; [2]USC;*
10:25-10:50	**Enabling High-Performance LPDDRx-Compatible MRAM** Jue Wang[1;] Xiangyu Dong[2]; Yuan Xie[1] *[1]Pennsylvania State University; [2]Qualcomm Technology, Inc.*	**Energy Harvesting from Anti-Corrosion Power Sources** Minseok Lee[1]; Kyeongsu Park[1]; Sehwan Kim[1]; Pai Chou[2] *[1]Dankook University; [2]University of California, Irvine*
10:50-11:15	**SBAC: A Statistics based Cache Bypassing Method for Asymmetric-access Caches** Chao Zhang[1]; Guangyu Sun[1]; Peng Li[2]; Tao Wang[1]; Dimin Niu[3]; Yiran Chen[4] *[1]Peking University; [2]UCLA; [3]Samsung Semiconductor Inc.; [4]University of Pittsburgh*	**Intelligent Frame Refresh for Energy-Aware Display Subsystems in Mobile Devices** Yongbing Huang[1,2]; Mingyu Chen[1]; Lixin Zhang[1]; Shihai Xiao[2]; Junfeng Zhao[2]; Zhulin Wei[2]; *[1]Chinese Academy of Sciences; [2]Huawei Technologies Co.*

ISLPED 2014 Program: Wednesday

11:15-11:40	**Tag Check Elision** Zhong Zheng[1]; Zhiying Wang[1]; Mikko Lipasti[2] *[1]National University of Defense Technology; [2]University of Wisconsin, Madison*	***(Invited paper)*** **Powering the Internet of Things** Hrishikesh Jayakumar, Kangwoo Lee, Woosuk Lee, Arnab Raha, Younghyun Kim, and Vijay Raghunathan *Purdue University*
11:40-12:00	**Break**	

Poster Papers

QPR.JS: A Runtime Framework for QoS-Aware Power Optimization for Parallel JavaScript Programs

Wonjun Lee[1,2]; Channoh Kim[2]; Houp Song[1]; Jae W. Lee[2];
[1]Samsung Electronics; [2]Sungkyunkwan University

Ultra-Low Voltage Mixed TFET-MOSFET 8T SRAM Cell

Yin-Nien Chen; Ming-Long Fan; Pi-Ho Hu; Pin Su; Ching-Te Chuang
National Chiao-Tung University

A-SAD: Power Efficient SAD Calculator for Real time H.264 Video Encoder Using MSB-Approximation Technique

Le Dinh Trang Dang; Ik Joon Chang; Jinsang Kim
Kyung Hee University

Design Exploration of Racetrack Lower-level Caches

Zhenyu Sun[1]; Xiuyuan Bi[2]; Alex K. Jones[2]; Hai Li[2]
[1]Broadcom Corp.; [2]University of Pittsburgh

A Compact Macromodel for the Charge Phase of a Battery with Typical Charging Protocol

Donghwa Shin[1]; Alessandro Sassone[2]; Alberto Bocca[2]; Alberto Macii[2]; Enrico Macii[2]; Massimo Poncino[2]
[1]Yeungnam University; [2]Politecnico di Torino

Energy Efficient Task Scheduling on a Multi-core Platform using Real-time Energy Measurements

Digvijay Singh; William Kaiser
University of California, Los Angeles

Energy-Efficient Mapping of Biomedical Applications on Domain-Specific Accelerator under Process Variation

Mohammad Khavari Tavana[1]; Amey Kulkarni[2]; Abbas Rahimi[3]; Tinoosh Mohsenin[2]; Houman Homayoun[1]
[1]George Mason University; [2]University of Maryland, Baltimore; [3]University of California, San Diego;

A Memory Rename Table to Reduce Energy and Improve Performance

Joseph Pusdesris; Benjamin VanderSloot; Trevor Mudge
University of Michigan

A Deterministic-Dither-Based, All-Digital System for On-Chip Power Supply Noise Measurement

Kannan Sankaragomathi; William Smith; Brian Otis; Visvesh Sathe
University of Washington

An Open-Source Framework for the Formal Specification and Simulation of Electrical Energy Systems

Sara Vinco[1]; Alessandro Sassone[1]; Franco Fummi[2]; Enrico Macii[1]; Massimo Poncino[1]
[1]Politecnico di Torino; [2]Universita' di Verona

Analysis and Optimization of In-Situ Error Detection Techniques in Ultra-Low-Voltage Pipeline

Seongjong Kim; Mingoo Seok
Columbia University

Quantifying the Impact of Variability on the Energy Efficiency for a Next-Generation Ultra-Green Supercomputer

Francesco Fraternali[1]; Andrea Bartolini[1]; Carlo Cavazzoni[2]; Giampietro Tecchiolli[3]; Luca Benini[1]
[1]University of Bologna; [2]Cineca; [3]Eurotech Group;

MIN: A Power Efficient Mechanism to Mitigate the Impact of Process Variations on Nanophotonic Networks

Majed Valad Beigi; Gokhan Memik
Northwestern university

EECache: Exploiting Design Choices in Energy-Efficient Last-Level Caches for Chip Multiprocessors

Hsiang-Yun Cheng; Matthew Poremba; Narges Shahidi ; Ivan Stalev; Mary Jane Irwin; Mahmut Kandemir; John Sampson; Yuan Xie
Pennsylvania State University

A Digital Dynamic Write Margin Sensor for Low Power Read/Write Operations in 28nm SRAM

Peter Beshay[1;] Vikas Chandra[2]; Rob Aitken[2]; Benton Calhoun[1]
[1]University of Virginia; [2]ARM;

Smart Butterfly: Reducing Static Power Dissipation of Network-on-Chip with Core-State-Awareness

Siyu Yue; Lizhong Chen; Di Zhu; Timothy Pinkston; Massoud Pedram
University of Southern California

Energy-Efficient Dot Product Computing using a Switched Analog Circuit Architecture

Ihab Nahlus[1]; Eric Kim[1]; Naresh Shanbhag[1]; David Blaauw[2]
[1]University Of Illinois Urbana Champaign; [2]University Of Michigan Ann-Arbor)

Gated low-Power Clock Tree Synthesis for 3D-ICs

Tiantao Lu; Ankur Srivastava
University of Maryland

Unlocking the True Potential of 3D CPUs with Micro-Fluidic Cooling

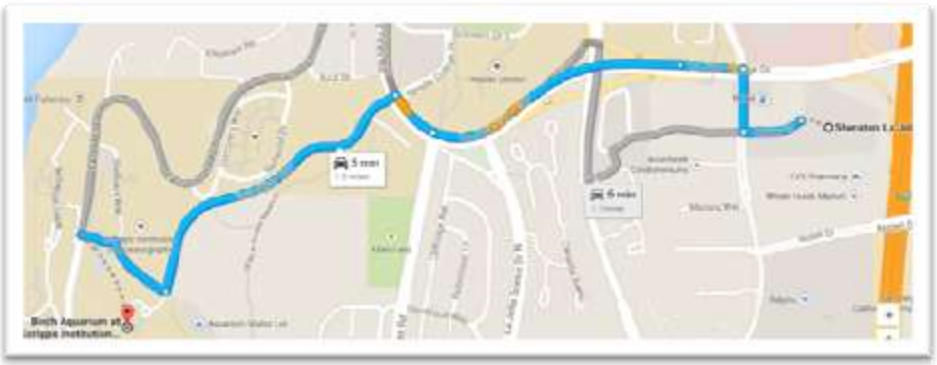
Caleb Serafy; Ankur Srivastava; Donald Yeung
University of Maryland, College Park

Prolonging PCM Lifetime through Energy-Efficient, Segment-Aware, and Wear-Resistant Page Allocation

Hoda Aghaei Khouzani; Yuan Xue; Archana Pandurangi; Chengmo Yang
University of Delaware

Maps: Sheraton La Jolla Hotel

Maps: Birch Aquarium from the Hotel



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