

Accept - Regular

ID	Title
22	Modeling and implementation of a fully-digital integrated per-core voltage regulation system in a 28nm high performance 64-bit processor
25	A Fully Parameterizable Low Power Design of Vector Fused Multiply-Add Using Active Clock-Gating Techniques
26	HiCAP: Hierarchical FSM-based Dynamic Integrated CPU-GPU Frequency Capping Governor for Energy-Efficient Mobile Gaming
34	Voltage Noise Induced DRAM Soft Error Reduction Technique for 3D-CPUs
46	In-place Repair for Resistive Memories Utilizing Complementary Resistive Switches
60	A Li-Ion Battery Charge Protocol with Optimal Aging-Quality of Service Trade-off
63	Therma: Thermal-aware Run-time Thread Migration for Nanophotonic Interconnects
68	TeleProbe: Zero-power Contactless Probing for Implantable Medical Devices
72	A light-powered, 'always on', smart camera with compressed domain gesture detection
75	ACAM: Approximate Computing Based on Adaptive Associative Memory with Online Learning
77	Energy-Efficient Programmable Analog-to-Information Converter for Biosignal Sensing
78	Bit Serializing a Microprocessor for Ultra-low-power
79	Prediction-Guided Performance-Energy Trade-off with Continuous Run-Time Adaptation
90	Adding Energy Dimension To Deep Neural Networks
96	Low Area, Low Power, Robust, Highly Sensitive Error Detecting Latch for Resilient Architectures
103	SATS: An Ultra-low Power Time Synchronization for Solar Energy Harvesting WSN
114	Domain Wall Memory based Convolutional Neural Networks for Bit-width Extendability and Energy-Efficiency
127	Ferroelectric Transistor based Non-Volatile Flip-Flop
129	An Energy Efficient PUF Design: Computing While Racing
130	Unified Power Frequency Model Framework
135	Reducing Power Consumption of GPGPUs through Instruction Reordering
136	Exploiting Fully Integrated Inductive Voltage Regulators to Improve Side Channel Resistance of Encryption Engines
139	On Effective and Efficient Quality Management for Approximate Computing
148	SocialHBC: Social Networking and Secure Authentication using Interference-Robust Human Body Communication
149	An Efficient Parallel Scheduling Scheme on Multi-partition PCM Architecture

163	Design and Implementation of a 4Kb STT-MRAM with Innovative 200nm Nano-ring Shaped MTJ
168	Power-Aware Performance Adaptation of Concurrent Applications in Heterogeneous Many-Core Systems
170	Soft Response Generation and Thresholding Strategies for Linear and Feed-Forward MUX PUFs
171	Performance Impact of Magnetic and Thermal Attacks on STTRAM and Low-Overhead Mitigation Techniques
173	Energy-Efficient Adaptive Classifier Design for Mobile Systems
181	Comprehensive Analysis, Modeling and Design for Hold-Timing Resiliency in Voltage Scalable Design
185	Analysis and Design of Energy Efficient Time Domain Signal Processing
195	DynSleep: Fine-grained Power Management for Latency-Critical Applications through Per-core Sleep States
198	An Energy-Efficient Computational Model for Uncertainty Management in Dynamically Changing Networked Wearables
199	An Energy-Aware Approach to Noise-Robust Moving Object Detection for Low-Power Wireless Image Sensor Platforms
204	Data-Driven Low-Cost On-Chip Memory with Adaptive Power-Quality Trade-off for Mobile Video Streaming
208	Scalable Auto-Tuning of Synthesis Parameters for Optimizing High-Performance Processors
210	Regenerative Breaking: Recovering Stored Energy from Inactive Voltage Domains for Energy-efficient Systems-on-Chip
212	Physical Design Solutions to Tackle FEOL/BEOL Degradation in Gate-level Monolithic 3D ICs
214	Four-tier Monolithic 3D ICs: Tier Partitioning Methodology and Power Benefit Study
217	A Robust and Energy-Efficient Classifier Using Brain-Inspired Hyperdimensional Computing
220	Speeding up Convolutional Neural Network Training with Dynamic Precision Scaling and Flexible Multiplier-Accumulator
231	Dynamic Approximation with Feedback Control for Energy-Efficient Recurrent Neural Network Hardware
248	Synthesis of Robust, near-V _{th} Asynchronous Circuits using Nell: an NCL Equation Language
252	Design and implementation of nonvolatile power-gating SRAM using SOTB technology