INTERNATIONAL SYMPOSIUM ON LOW POWER ELECTRONICS AND DESIGN 2004

http://www.islped.org

Newport Beach Marriott Hotel, Newport, California

ADVANCE PROGRAM

MONDAY, August 9, 2004

7:15-8:15 Breakfast (Atrium room)

8:15-8:30 Opening Welcome (salon C/D)

Welcome Message
Rajiv Joshi, Kiyoung Choi, General Co-Chairs

Symposium Highlights
Vivek Tiwari, Kaushik Roy, TPC Co-Chairs

8:30-9:30 Keynote Talk (salon C/D): *Why Hot Chips Are No Longer "Cool"*

Ray Bryant, Director of PowerPC Products, IBM Systems & Technology Group

9:30-9:45 Break

9:45-11:10 Session 1 (Salon C): Circuit Challenges for Scaled Technologies

Session Chair: Takayasu Sakurai, Univ. of Tokyo
Co-Chair: Wei Hwang, National Chiao Tung Univ.

1.1 *Leakage Power Reduction by Dual-Vth Designs under Probabilistic Analysis of Vth Variation*
Michael Liu, Wei-Shen Wang, Michael Orshansky, Univ. of Texas, Austin

1.2 *Larger-than-Vdd Forward Body Bias in sub-0.5V Nanoscale CMOS*
Hari Ananthan, Purdue Univ., Chris H. Kim, Kaushik Roy

1.3 *Technology Exploration for Adaptive Power and Frequency Scaling in 90nm CMOS*
Maurice Meijer, Philips, Francesco Pessolano, José Pineda de Gyvez

1.4 *Experimental Measurement of A Novel Power Gating Structure with Intermediate Power Saving Mode*
Suhwan Kim, Seoul National University, Korea, Daniel R. Knebel, Stephen V. Kosonocky, Kevin Stawiasz

9:45-11:10 Session 2 (Salon D): Microarchitectural Techniques for Power Reduction

Session Chair: Mary Jane Irwin, Pennsylvania State Univ.
Co-Chair: Trevor Mudge, Univ. of Michigan

2.1 *Improved Clock-Gating through Transparent Pipelining*
Hans M. Jacobson, IBM

2.2 *Microarchitectural Techniques for Power Gating Execution Units*
Zhigang Hu, IBM, Alper Buyuktosunoglu, Viji Srinivasan, Victor Zyuban, Hans Jacobson, Pradip Bose

2.3 *SEPAS: A Highly Accurate Energy-Efficient Branch Predictor*
Amirali Baniasadi, Univ. of Victoria, B.C., Andreas Moshovos

2.4 *Understanding the Energy Efficiency of Simultaneous Multithreading*
Yingmin Li, Univ. of Virginia, David Brooks, Zhigang Hu, Kevin Skadron, Pradip Bose

11:10-11:30 Break

11:30-12:30 Poster Session 1 (Salon C): Cache and Bus Design

Session Chair: Mahadev Nemani, Intel Corp.

1.1p *Impact of Technology Scaling on Energy Aware Execution Cache-based Microarchitectures*
Emil Talpes, CMU, Diana Marculescu

1.2p Single-VDD and Single-VT Super-Drowsy Techniques for Low-Leakage High-Performance Instruction Caches
Nam Sung Kim, Intel Corp., Trevor Mudge

1.3p *Design and Implementation of Correlating Caches*
Arindam Malik, Northwestern Univ., Gokhan Memik

1.4p *Dynamic Power Management for Streaming Data*
Nathaniel Pettis, Purdue Univ., Le Cai, Yung-Hsiang Lu

1.5p *Delayed Line Bus Scheme: A Low-Power Bus Scheme for Coupled On-Chip Buses*
Maged Ghoneima, Northwestern Univ. , Yehea Ismail

11:30-12.30 Poster Session 2 (Salon D): System Design Methodologies

Session Chair: Yung-Hsiang Lu, Purdue Univ.

2.1p *Delay Optimal Low-Power Circuit Clustering for FPGAs with Dual Supply Voltages*
Deming Chen, Jason Cong, UCLA

2.2p *Creating a Power-aware Structured ASIC*
R. Reed Taylor, CMU, Herman Schmit

2.3p *Dynamic Voltage Scaling Techniques for System-wide Energy Minimization in Real Time Embedded Systems*
Ravindra Jejurikar, UC Irvine, Rajesh K. Gupta

2.4p *ESACW: An Adaptive Algorithm For Transmission Power Reduction in Wireless Networks*
Hang Su, Peiliang Qiu, Qinru Qiu, State Univ. of NY

2.5p *Any-time Probabilistic Switching Model using Bayesian Networks*
Shiva Shankar Ramani, Sanjukta Bhanja, Univ. of South Florida

12:30-14:00 Lunch (Atrium room)

14:00-15:25 Session 3 (Salon C): Technologies and Devices for Low-Power

Session Chair: Tom Burd
Co-Chair: Ali Keshavarzi, Intel Corp.

3.1 *Characterizing and Modeling Minimum Energy Operation for Subthreshold Circuits*
Benton H. Calhoun, MIT, Anantha Chandrakasan

3.2 *Device Optimization for Ultra-Low Power Digital Sub-threshold Operation*
Bipul Paul, Purdue Univ., Arijit Raychwdhury, Kaushik Roy

3.3 *Nanoscale CMOS Circuit Leakage Power Reduction by Double-Gate Device*
Keunwoo Kim, IBM, Koushik K. Das, Rajiv V. Joshi, Ching-Te Chuang

3.4 *4T-Decay Sensors: A New Class of Small, Fast, Robust, and Low-Power, Temperature/Leakage Sensors*
Stefanos Kaxiras, Univ. of Patras, Greece, Polychronis Xekalakis

14:00-15:25 Session 4 (Salon D): Power Optimizations for Cache Memory

Session Chair: Renu Mehra, Synopsys
Co-Chair: Dinesh Somasekhar, Intel Corp.

4.1 *Hotspot Cache: Joint Temporal and Spatial Locality Exploitation for I-Cache Energy Reduction*
Chia-lin Yang, Nat'l Taiwan Univ., Taipei, Taiwan, Chien-hao

4.2 *Location Cache: A Low-Power L2 Cache System*
Rui Min, Univ. of Cincinnati, Yiming Hu, Wen-ben Jone

4.3 *A Way-Halting Cache for Low-Energy High-Performance Systems*
Chuanjun Zhang, UC, Riverside, Frank Vahid, Jun Yang, Walid Najjar

4.4 *Soft Error and Energy Consumption Interactions: A Data Cache Perspective*
N.Vijaykrishnan, Penn State Univ., Vijay Degalahal, Lin Li, Mahmut Kandemir, Mary Jane Irwin

15:25-15:45 Break

15:45-17:10 Session 5 (Salon C): Leakage Analysis and Optimization

Session Chair: Massoud Pedram, USC
Co-Chair: Wolfgang Nebel, OFFIS

5.1 A Methodology for Post-Layout Leakage Power Minimization Based on Distributed Sleep Transistor Insertion

Pietro Babighian, Luca Benini, Alberto Macii, Enrico Macii, Politecnico di Torino, Antonio Remollino

5.2 *Total Power Optimization through Simultaneously Multiple-VDD Multiple-VTH Assignment and Device Sizing with Stack Forcing*

Wei-Lun Hung, Yuan Xie, Penn State Univ.,Vijaykrishnan Narayanan, Mahmut Kandemir, Mary Jane Irwin

5.3 *Active Mode Leakage Reduction Using Fine-Grained Forward Body Biasing Strategy*

Vishal Khandelwal, Univ. of Maryland, Ankur Srivastava

5.4 *A Probabilistic Framework to Estimate Full Chip subthreshold Leakage Power Distribution Considering Within-Die and Die-to-Die P-T-V Variations*

Songqing Zhang, Vineet Wason, UC Santa Barbara, Kaustav Banerjee

15:45-17:10 Session 6 (Salon D): Power Supply, Voltage, and Frequency Management

Session Chair: Rajesh Gupta, UC, San Diego
Co-Chair: Massimo Poncino, Universita Di Verona

6.1 *Maximizing Efficiency of Solar-Powered Systems by Load Matching*

Dexin Li, UC Irvine, Pai H. Chou

6.2 *Power Utility Maximization for Multiple-Supply Systems by a Load-Matching Switch*

Chulsung Park, UC Irvine, Pai H. Chou

6.3 *Dynamic Voltage and Frequency Scaling based on Workload Decomposition*

Kihwan Choi, USC., Ramakrishna Soma, Massoud Pedram

6.4 *Architecting Voltage Islands in Core-based System-on-a-Chip Designs*

Jingcao Hu, Youngsoo Shin, IBM, Nagu Dhanwada, Radu Marculescu

5:10-6:00 Invited Talk: *Balancing Energy Optimization*

John Cornish, Director of Product Marketing, ARM Corporation

TUESDAY, August 10, 2004

7:15-8:15 Breakfast (Atrium room)

8:30-9:30 Plenary Talk I (salon C/D): *Battery Life Challenges on Future Mobile Notebook Platforms*

Shreekant (Ticky) Thakkar, Director, Mobile Platform Architecture, Intel Corp.

9:30-9:45 Break

9:45-11:10 Session 7 (Salon C): Power-efficient Bus Design

Session Chair: Youngsoo Shin, Korea Advanced Inst. of Science and Tech
Co-Chair: Nagu Dhanwada, IBM

7.1 A*pproaches to Run-time and Standby Mode Leakage Reduction in Global Buses*

Rahul Rao, Univ of Michigan, Kanak Agarwal, Dennis Sylvester, Richard Brown, Kevin Nowka, Sani Nassif

7.2 *Spatial Encoding Circuit Techniques for Peak Power Reduction of On-Chip High-Performance Buses*

Himanshu Kaul, Univ of Michigan, Dennis Sylvester, Mark Anders, Ram Krishnamurthy

7.3 *A New Algorithm for Improved VDD Assignment in Low Power Dual VDD Systems*

Sarvesh H Kulkarni, Univ of Michigan, Ashish N Srivastava, Dennis Sylvester

7.4 *Limited Intra-Word Transition Codes: An Energy-Efficient Bus Encoding for LCD Display Interfaces*

Alberto Bocca , Sabino Salerno, Enrico Macii, Massimo Poncino, Universita' di Verona

9:45-11:10 Session 8 (Salon D): High Level Power Modeling and Analysis

Session Chair: David Brooks, Harvard Univ.
Co-Chair: Joerg Henkel, University of Karlsruhe

8.1 *Microarchitectural Power Modeling Techniques for Deep Sub-Micron Microprocessors*

Nam Sung Kim, Intel Corp., Taeho Kgil, Valeria Vertaco, Todd Austin, Trevor Mudge

8.2 *Power-Optimal Pipelining in Deep Submicron Technology*

Seongmoo Heo, MIT, Krste Asanovic

8.3 *Application-Level Prediction of Battery Dissipation*

Chandra J. Krintz, UC Santa Barbara, Ye Wen, Rich Wolski

8.4 *Minimizing power consumption and complexity in a programmable transmit filter bank for OFDM*

Alireza Mehrnia, UCLA, Babak Daneshrad

11:10-11:30 Break

11:30-12:30 Poster Session 3 (Salon C): Circuit Technologies

Session Chair: Yehea Ismail, Northwestern Univ

3.1p *On Optimality of Adiabatic Switching in MOS Energy-Recovery Circuits*

Baohua Wang, Pinaki Mazumder, Univ of Michigan

3.2p *Constant-Load Energy Recovery Memory for Efficient High Speed Operation*

Joohee Kim, Univ of Michigan, Marios C. Papaefthymiou

3.3p *A Comparative Study of MOS VCOs for Low Voltage High performance Operation*

Jing-Hong Conan Zhan, Cornell Univ., Jon. S. Duster, Kevin. T. Kornegay

3.4p *A CPL-based Dual Supply 32-bit ALU for Sub 180nm CMOS Technologies*

B. Chatterjee, Univ. of Waterloo, Canada, M. Sachdev, R. Krishnamurthy

11:30-12:30 Design Contest Presentations (Salon D)

Session Chair: David Scott, Texas Instruments

1d *DuraNode: Wireless Sensor for Structural Health Monitoring*

Chulsung Park, UC Irvine, Qiang Xie, Pai H. Chou

2d *Eco: an Ultra-Compact Low-Power Wireless Sensor Node for Real-Time Motion Monitoring*

Chulsung Park, UC Irvine, Jinfeng Liu, and Pai H. Chou

3d *An Application-Transparent Backlight Power Management Framework for a Transflective TFT LCD*

Hojun Shim, Seoul Natl. U, S Korea , Naehyuck Chang, Massoud Pedram

4d *A 0.5-V 0.25-mm 32-b RISC Core*

Hung-Yu Li, Chung Cheng Univ., Taiwan, Chao-Ching Wang, Jinn-Shyan Wang

12:30-14:00 Lunch (Atrium room)

14:00-15:25 Session 9 (Salon C): Low Power Converter Circuits

Session Chair: Dr. Remus Albu, Philips Research.
Co-Chair: Gu-Yeon Wei, TPC, Harvard

9.1 *A Low power Rail to rail 6-Bit Flash ADC Based on a Novel Complimentary Average-Value Approach*

Hui-Chin Tseng , Hsin-Hung Ou, Chi-Sheng Lin and Bin-Da Liu, Natl. Cheng Kung Univ., Tainan, Taiwan

9.2 I*ntegrated Adaptive DC/DC Conversion with Adaptive Pulse-Train Technique for Low-Ripple Fast-Response Regulation*

Chuang Zhang, Louisiana State Univ.,Dongsheng Ma and Ashok Srivastava

9.3 *Feasibility of Monolithic and 3D-Sstacked DC-DC Converters for Microprocessors 90nm Technology Generation*

Gerhard Schrom, Intel Corp., Peter Hazucha, Jae-Hong Hahn, Volkan Kursun, Donald Gardner, Siva Narendra, Tanay Karnik, Vivek De

9.4 *2.45 GHz Power and Data Transmission for a Low-Power Autonomous Sensors Platform*

Stefano Gregori, Yunlei Li, Huijuan Li, Jin Liu, UT Dallas Franco Maloberti

14:00-15:25 Embedded Tutorial 1 (Salon D): *Managing Standby and Active Mode Leakage Power in Deep Sub-micron Design*

Larry Clark, Univ of New Mexico; Rakesh Patel, Intel Corp

15:25-15:45 Break

15:45-17:10 Session 10 (Salon C): Circuits for Low Power Wireless

Session Chair: Won Namgoong, USC
Co-Chair: Payam Heydari, UC Irvine

10.1 *Architectures for Low Power Ultra-Wideband Impulse Radio Receivers in the 3.1-5GHz band*

M. Verhelst, Katholieke Univ. Leuven, Belgium, W. Vereecken, M. Steyaert, W. Dehaene

10.2 *Low Power Asynchronous Viterbi Decoder for Wireless Applications*

Mohamed Kawokgy, Univ. of Toronto, Canada, C. André T. Salama,

10.3 *A CMOS Even Harmonic Mixer With Current Reuse for Low Power Applications*
Ming-Feng Huang, Natl. Chung Cheng Univ., Taiwan**,** Shuenn-Yuh Lee, Chung J. Kuo.
10.4 *A Novel Continuous-Time Common Mode Feedback for Low-Voltage Switched-OPAMP*
Mohammad Ali-Bakhshian, Sharif University of Technology, Iran, Khosrow Sadeghi

15:45-17:10 Session 11 (Salon D): Power Efficient Design for Arithmetic Circuits
Session Chair: Krste Asanovich, MIT
Co-Chair: Vamsi Srikantam, Agilent Labs

11.1 *The Design of a Low Power Asynchronous Multiplier*
Yijun Liu, Univ. of Manchester, UK**,** Steve Furber
11.2 *Low-Power Fixed-Width Array Multipliers*
Jinn-Shyan Wang, Natl. Chung Cheng Univ, Taiwan, Chien-Nan Kuo, Tsung-Han Yang
11.3 *Low-Power Carry-Select Adder Using Adaptive Supply Voltage Based on Input Vector Patterns*
Hiroaki Suzuki, Purdue Univ**.**, Woopyo Jeong, Kaushik Roy
11.4 *Reducing Pipeline Energy Demands with Local DVS and Dynamic Retiming*
Seokwoo Lee, Univ. of Michigan, Todd Austin, David Blaauw, Trevor Mudge

18:00-21:00 Banquet (California Ballroom)

WEDNESDAY, August 11, 2004

7:15-8:15 Breakfast (Atrium room)

8:30-9:30 Plenary Speech II (salon C/D): *Understanding Nanoscale Conductors*
Prof. Supriyo Datta, Purdue University

9:30-9:45 Break

9:45-11:10 Session 12 (Salon C): Energy Efficient Architectural Techniques
Session Chair: Victor Zyuban, IBM
Co-Chair: Pai Chou, UC, Irvine

12.1 *Eliminating Voltage Emergencies via Microarchitectural Voltage Control Feedback and Dynamic Optimization*
Kim Hazelwood, Harvard Univ**.**, David Brooks
12.2 *Mitigating Inductive Noise in SMT Processors*
Wael El-Essawy, Univ. of Rochester, David H. Albonesi
12.3 *Energy-Aware Demand Paging on NAND Flash-based Embedded Storages*
Chanik Park**,** Junguk Kang, Advanced Inst. of Sc. and Tech., Korea**,** Sunyoung Park, Jinsoo Kim
12.4 *Application Adaptive Energy Efficient Clustered Architectures*
Diana Marculescu, CMU

9:45-11:10 Embedded Tutorial 2 (Salon D): *The Impact of Variability on Power*
Sani Nassif, IBM Austin Research Laboratory

11:10-11:30 Break

11:30-12:30 Session 13 (Salon C): Wireless Application Drivers for Low-Power Systems
Session Chair: Sujit Dey, UCSD
Co-Chair: Diana Marculescu, CMU

13.1 *Reducing Energy Consumption of Key Management Protocols for Wireless Sensor Networks*
Bocheng Lai, UCLA**,** David D. Hwang, Ingrid Verbauwhede
13.2 *Evaluating and Optimizing Power Consumption of Anti-Collision Protocols for Applications in RFID Systems*
Feng Zhou, Fudan Univ., Sanghai, China, Chunhong Chen
13.3 *Experience with a low power wireless mobile computing platform*
Vijay Raghunathan, UCLA, Trevor Pering, Roy Want, Alex Nguyen, Peter Jensen
13.4 *FSM–Based Power Modeling of Wireless Protocols: the Case of Bluetooth*
Luca Negri, Politecnico di Milano, Italy, Mariagiovanna Sami, David Macii, Alessandra Terranegra

11:30-12:30 Session 14 (Salon D): Adaptive Voltage Scaling
Session Chair: Qing Wu, SUNY Binghampton
Co-Chair: Trevor Pering, Intel Corp.

14.1 *Efficient Adaptive Voltage Scaling System through On-Chip Critical Path Emulation*
Mohamed Elgebaly, Univ. of Waterloo, Canada, Manoj Sachdev
14.2 *An Efficient Voltage Scaling Algorithm for Complex SoCs with Few Number of Voltage Modes*
Bita Gorji-ara, UC Irvine, Pai Chou, Nader Bagherzadeh
14.3 *Memory-Aware Energy-Optimal Frequency Assignment for Dynamic Supply Voltage Scaling*
Youngjin Cho, Naehyuck Chang, Seoul National University, Korea
14.4 *Preemption-Aware Dynamic Voltage Scaling in Hard Real-Time Systems*
Woonseok Kim, Jihong Kim, Seoul Natl Univ., Korea, Sang Lyul Min

Closing Remarks

Space for ACM Mailer Information