



# Low Power Design

*From Technology Challenges to Great Products*

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# Agenda

Is power really a problem?

Are there viable solutions? What are the challenges to use them?

Designing low-power products

Conclusions



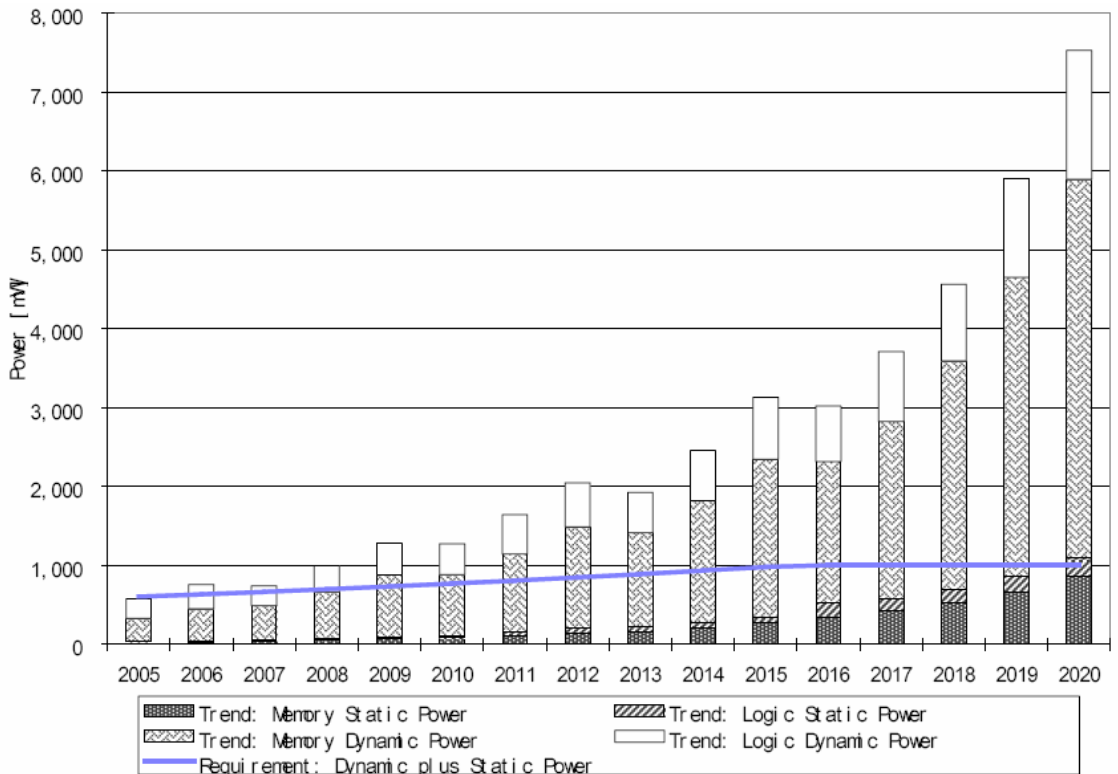
**Is power really a problem?**

# Scaling increases power more than expected

- ▶ CMOS 65nm technology represents a real challenge for any sort of voltage and frequency scaling
  - Supply voltages stable at 1.2v
- ▶ Starting from 120nm, each new process has inherently higher dynamic and leakage current density with minimal speed advantage
  - 90nm to 65nm: same dynamic power and ~5% higher leakage/mm<sup>2</sup>
- ▶ Low cost continues to drive higher levels of integration
- ▶ Low cost technological breakthroughs to keep power under control are getting very scarce
  - Examples: changing device or tuning the process to the application

# Modern SoC's demand more power

- ▶ Logic:
  - Static power is growing really fast
  - Dynamic power kind of grows
- ▶ Memory
  - Static power is growing really fast
  - Dynamic power kind of grows
- ▶ Overall power is dramatically increasing



*"Power-Efficient System-on-Chip power Trends, System Drivers", International Technology Roadmap for Semiconductors (ITRS) 2005*

# But, do we need to bother with power?

- ▶ The **mobile device** consumer demands more features and extended battery life at a lower cost
  - About 70% of users rate longer talk and stand-by time as primary mobile phone feature
  - Top 3G requirement for operators is power efficiency
- ▶ Customers want **smaller, sleeker mobile devices**
  - Requires this high levels of Silicon integration in advanced processes, but ...
  - Advanced processes have inherently higher leakage current
- ▶ Therefore, **we do need to bother with reducing power!**

# Increasing the Challenge; conflicting requirements

- ▶ Low **cost is always critical** in the consumer market
  - Cannot afford exotic packaging to solve power consumption issues
  - Products must consume less power
- ▶ Home consumers want products that **enhance the user experience**
  - Reduced noise (no fans)
  - Environmental issues
- ▶ When **docking mobile devices** for in-home use, consumers expect the same performance as tethered products
  - Relief from device battery life constraints
  - Products must be able to deliver high performance when docked

**Thus, is power really a problem?**

**Yes**

Power is a problem

& the user needs increase the challenge !!!



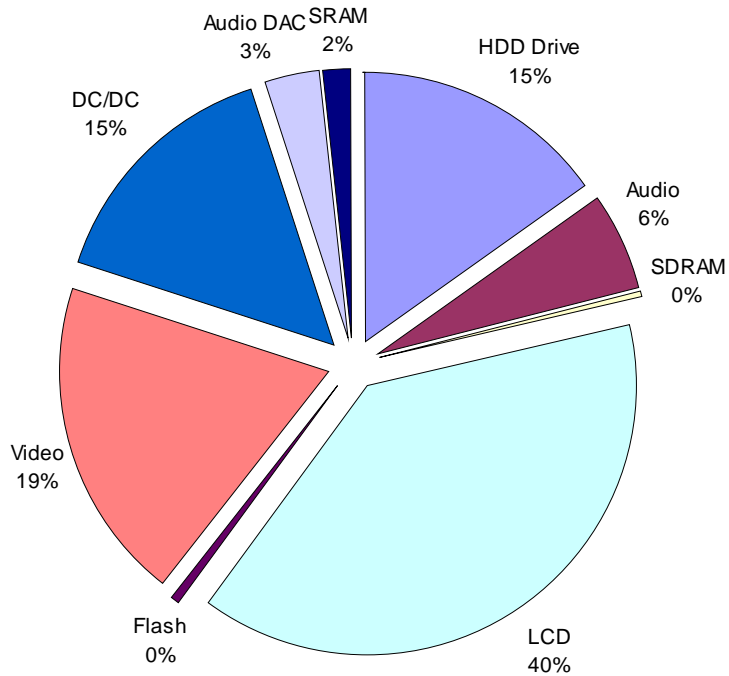


**What can we do?**

# An holistic approach for a pervasive problem

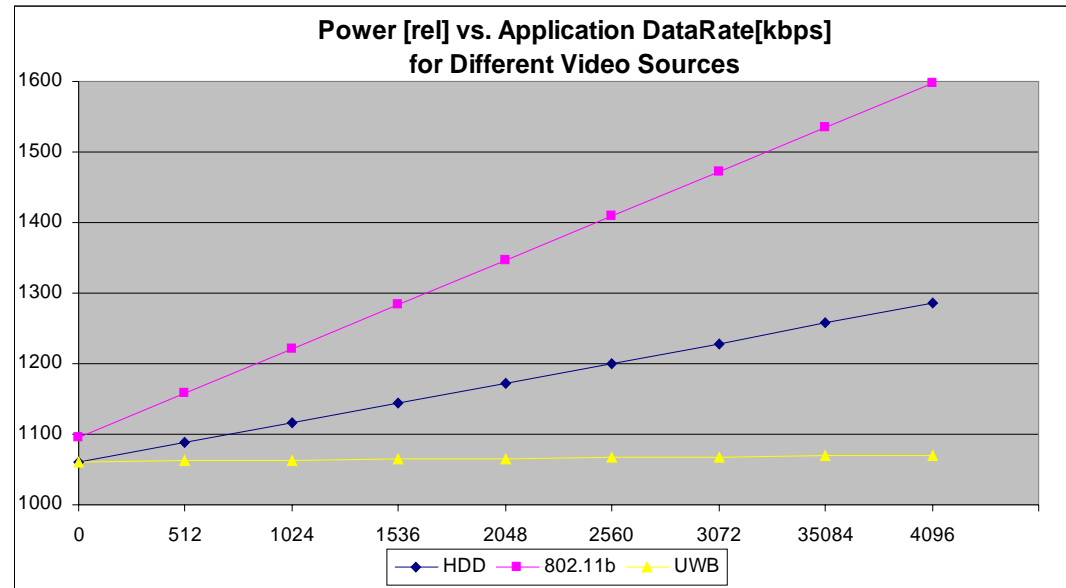
- ▶ Low Power requires an **holistic approach** across many areas
  - **System solutions**: Software power management control, OS and Firmware, instruction set extensions, power management devices
  - **SoC design technologies**: Optimized processors, voltage and frequency scaling, design architectures, tools and flows, quality of service
  - **Low-power building blocks**: Ultra low power processes, low power IP, advanced packaging strategies
- ▶ A product conception and design team need **expertise and solutions** in all these areas
- ▶ Each partner in the production/supply chains need **expertise and solutions** in all these areas
- ▶ Unfortunately, **low-power solutions** normally conflict with the low-cost requirement

# Holistic approach: system first



Identify where to act !!!

## Understand the trade-offs



# Holistic approach: define the problem

$$P = (1 - AF) P_{\text{idle}} + AF \cdot P_{\text{dynamic}}$$

Optimization space

Application dependent !!!

# Holistic approach: $AF < 50\%$

- ▶ The system is mostly idle. Thus, minimize stand-by power!
  - For example: pagers and mobile phones.
- ▶ Minimize software activity in stand-by
  - Make stand-by a real stand-by
- ▶ Switch off power from unused modules, ICs and cores
  - Use MSV or similar techniques
- ▶ Use high  $V_t$  to minimize  $I_{off}$ 
  - Minimize the intrinsic leakage
- ▶ Choose a process with a high  $I_{on}/I_{off}$  ratio
  - Basically any currently named Low Power process should do

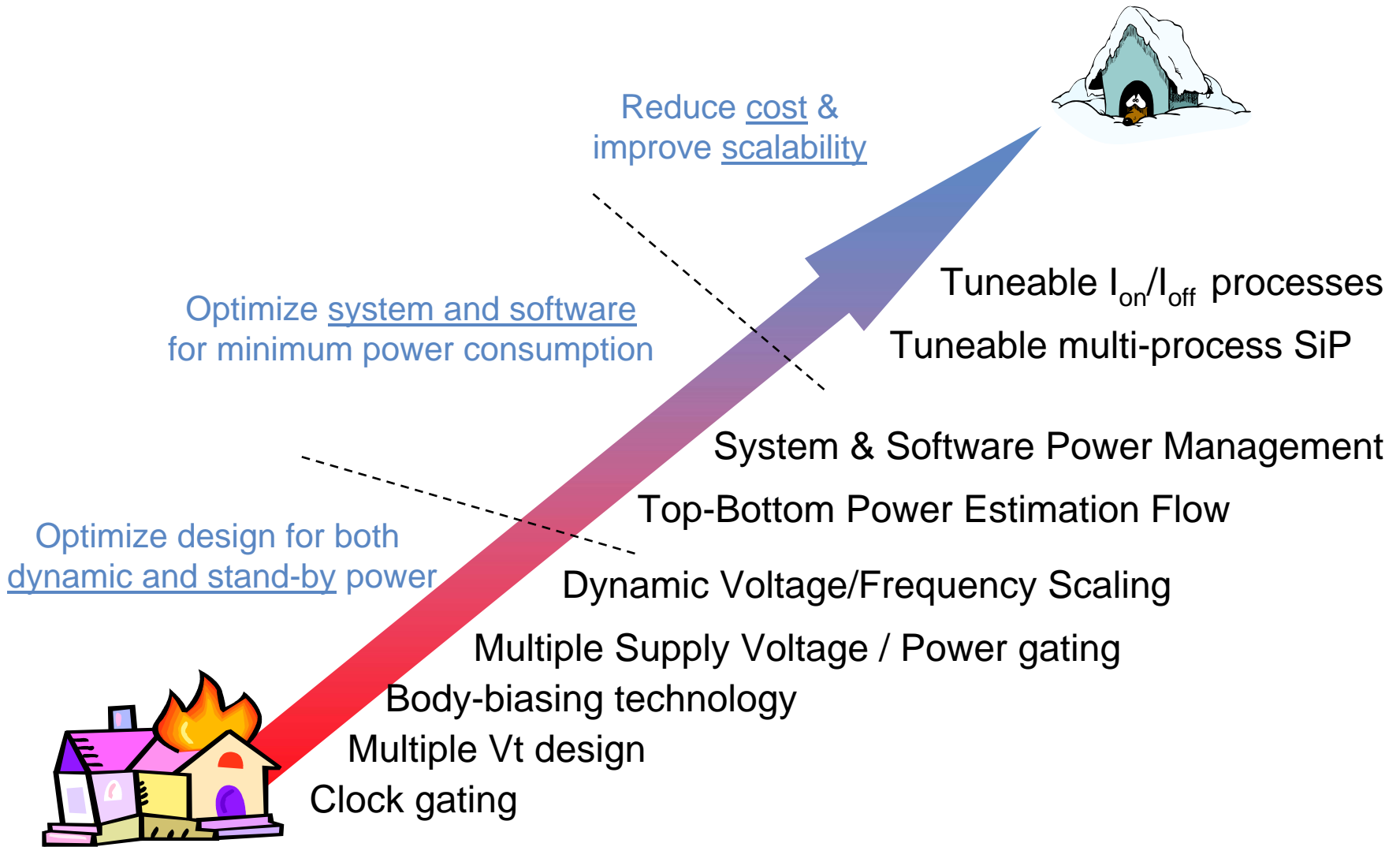
# Holistic approach: $AF > 50\%$

- ▶ The system is mostly active. Thus, minimize dynamic power!
  - For example: DVD players, Sony PSP, etc.
- ▶ Use Software Power Manager to use just-enough performance and power
  - Do not waste performance when not needed.
- ▶ Make your system adaptive (e.g. voltage/frequency scaling) according to the nature of your application
  - Use all the time every task has to complete.
- ▶ Choose low-power IOs, memories, libraries, etc.
- ▶ Use a multiple-Vt design style and clock gating.
- ▶ Choose a process with a low  $I_{on}/I_{off}$  ratio
  - This is not what is typically called an LP process!!!

# Holistic approach: AF ~ 50%

- ▶ The system behavior is not constant. It's the low power nightmare!
  - For example: a pocket PC or a Smartphone (used as such)
- ▶ Make your **system really adaptable** using aggressive voltage/frequency scaling, back biasing and a process with tunable  $I_{on}/I_{off}$  ratio coupled with Software Power Management wherever possible!
- ▶ Use prediction of the system loading to better tune it.
- ▶ Final power budget **will be worse** when comparing the same function in such a system **with respect to the previous two cases!!!**

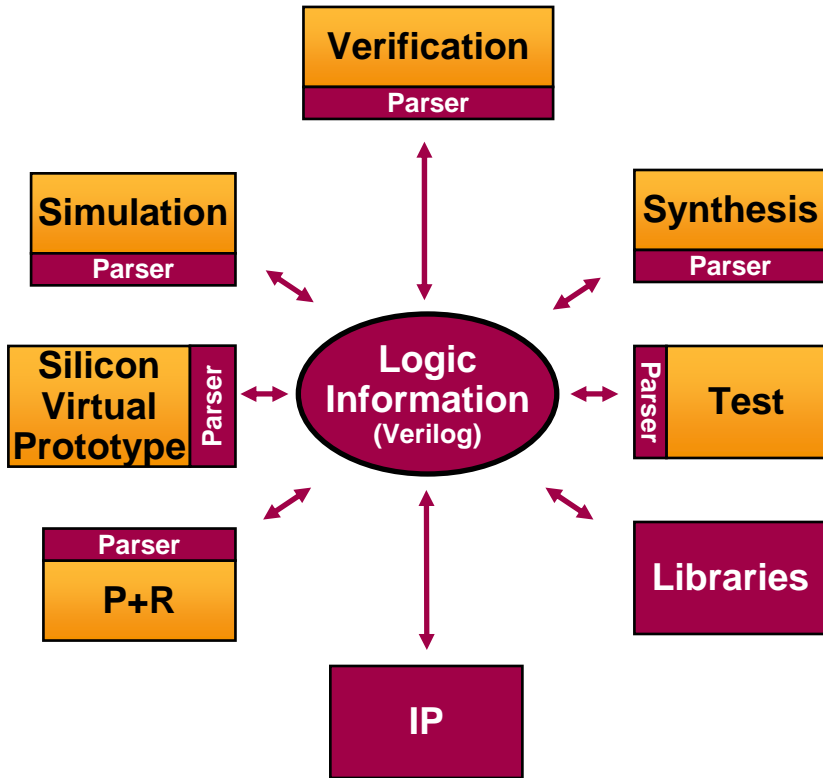
# Holistic approach: solution space





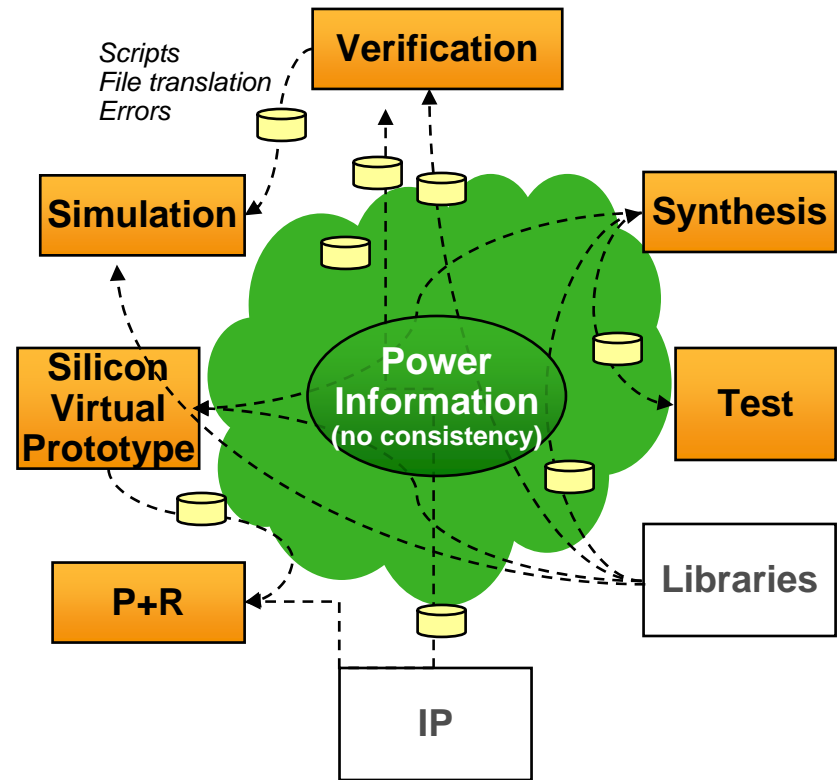
# Holistic approach: design technologies ?

Logic is “Connected”



Can be Automated

Power is Not “Connected”



Very Difficult to Automate

# Holistic approach needs co-operation!

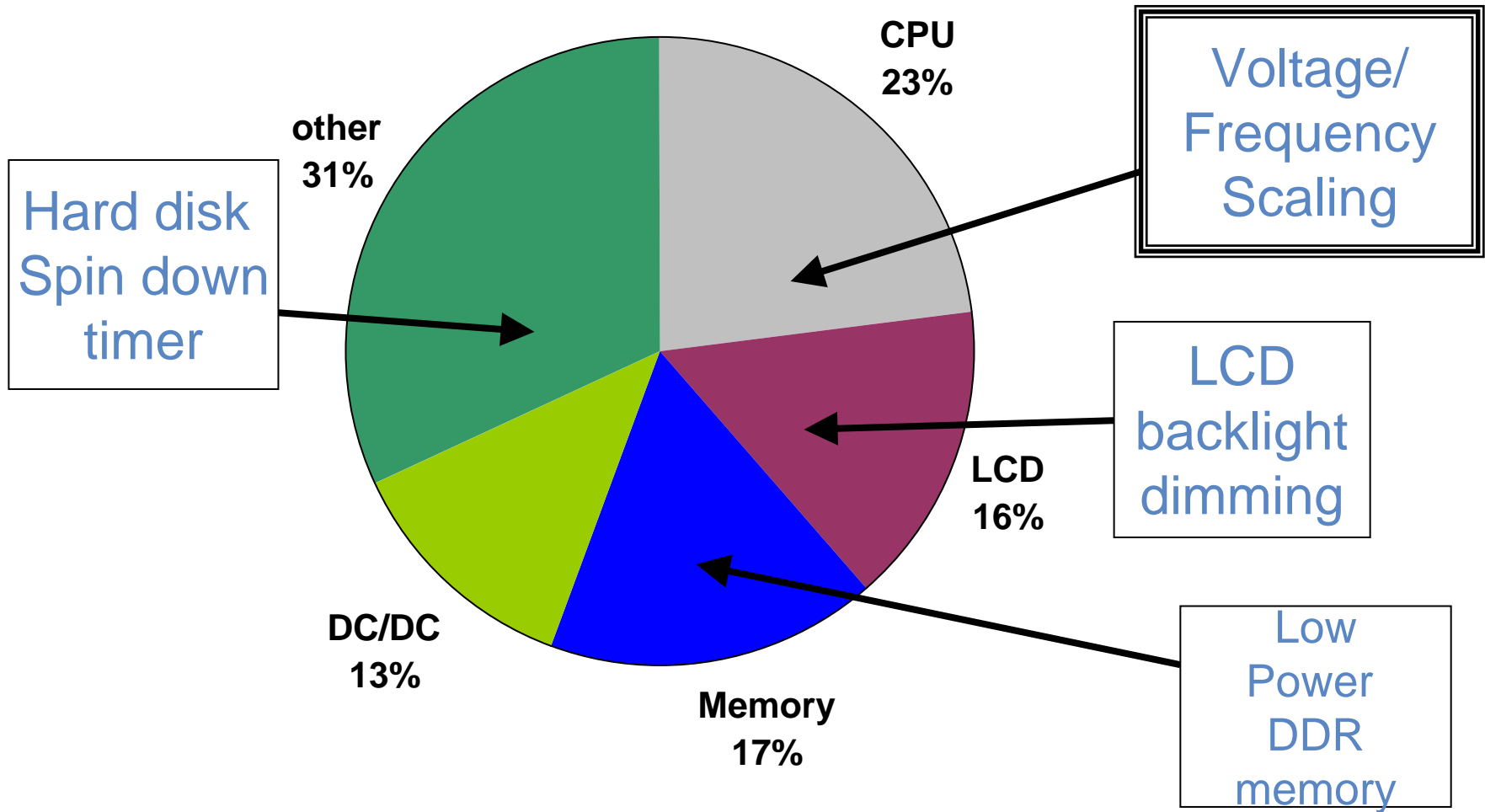


Is this an opportunity  
for collaboration or an  
area in which to  
compete ?

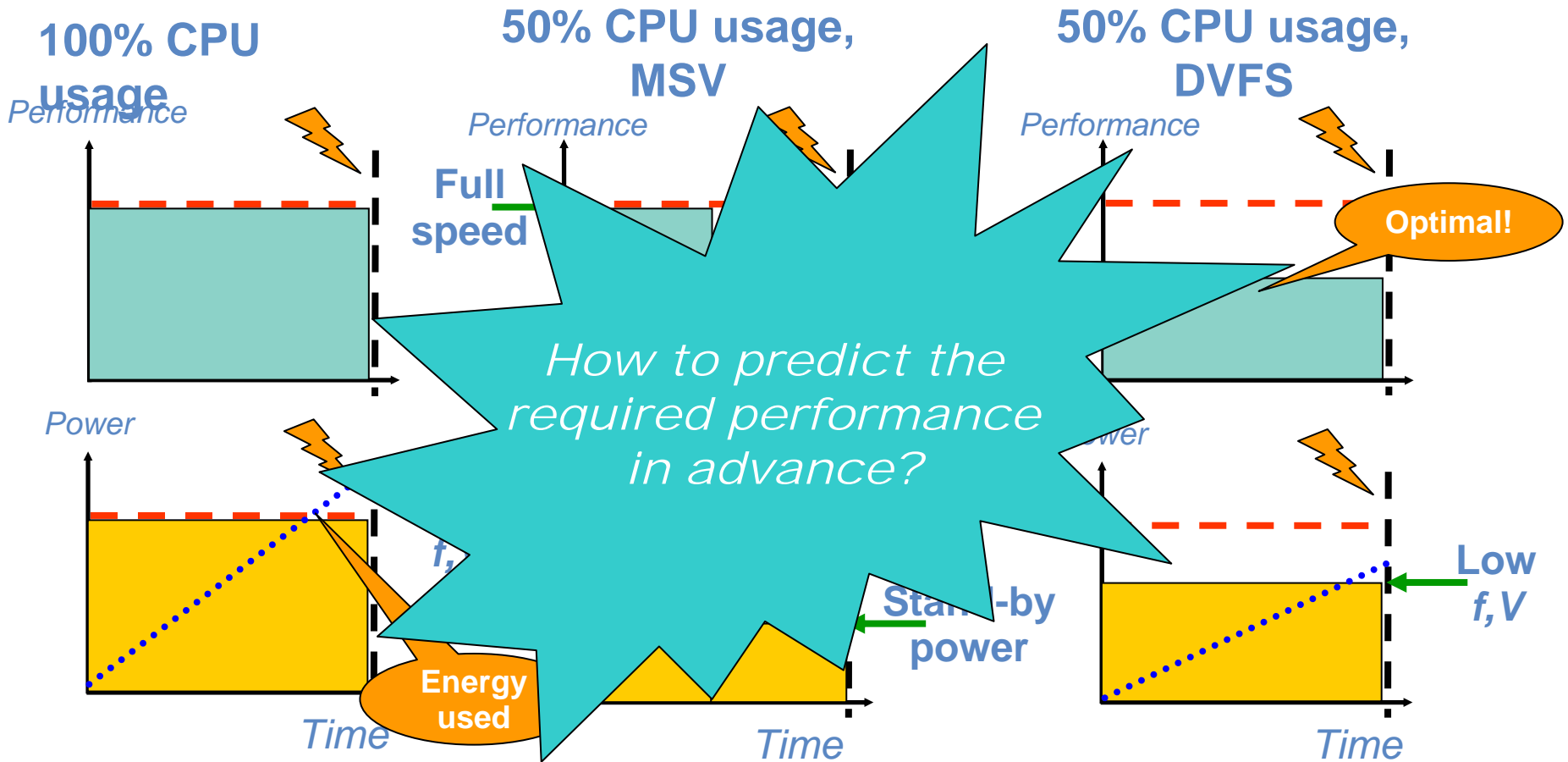


# Low-power design: eChip

# Starting from the system issues



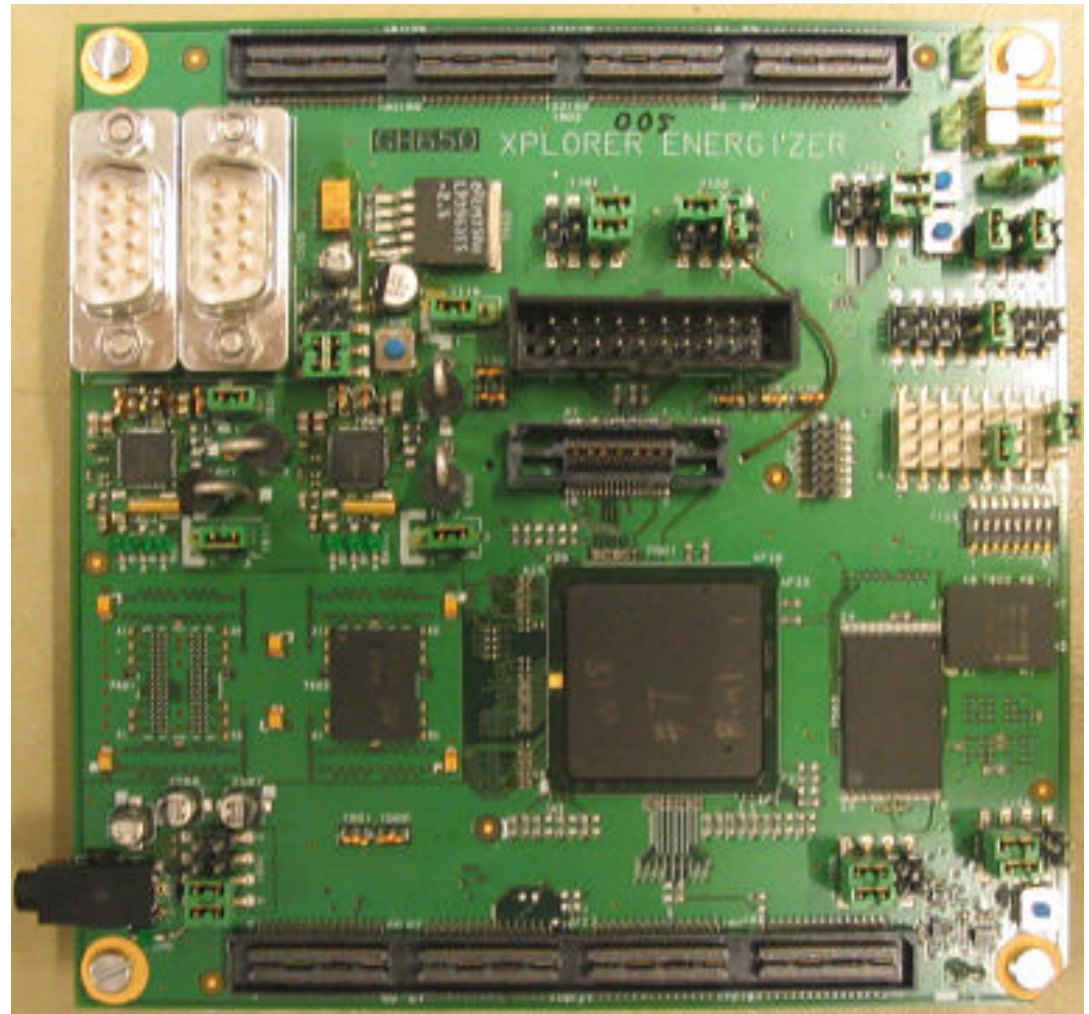
# Voltage/Frequency Scaling basics



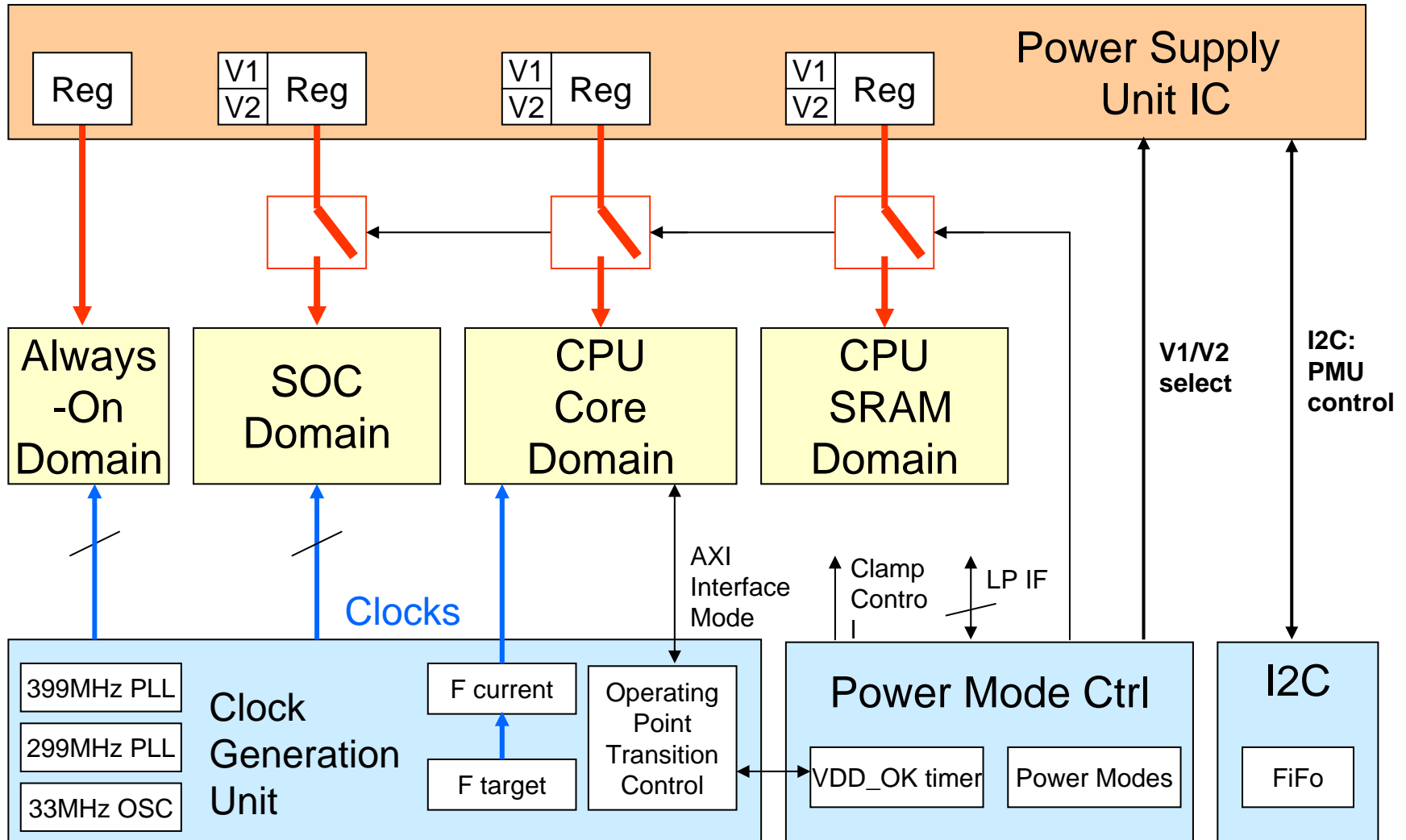
Power savings are achieved by executing a workload at a lower frequency.

# eChip: Block diagram

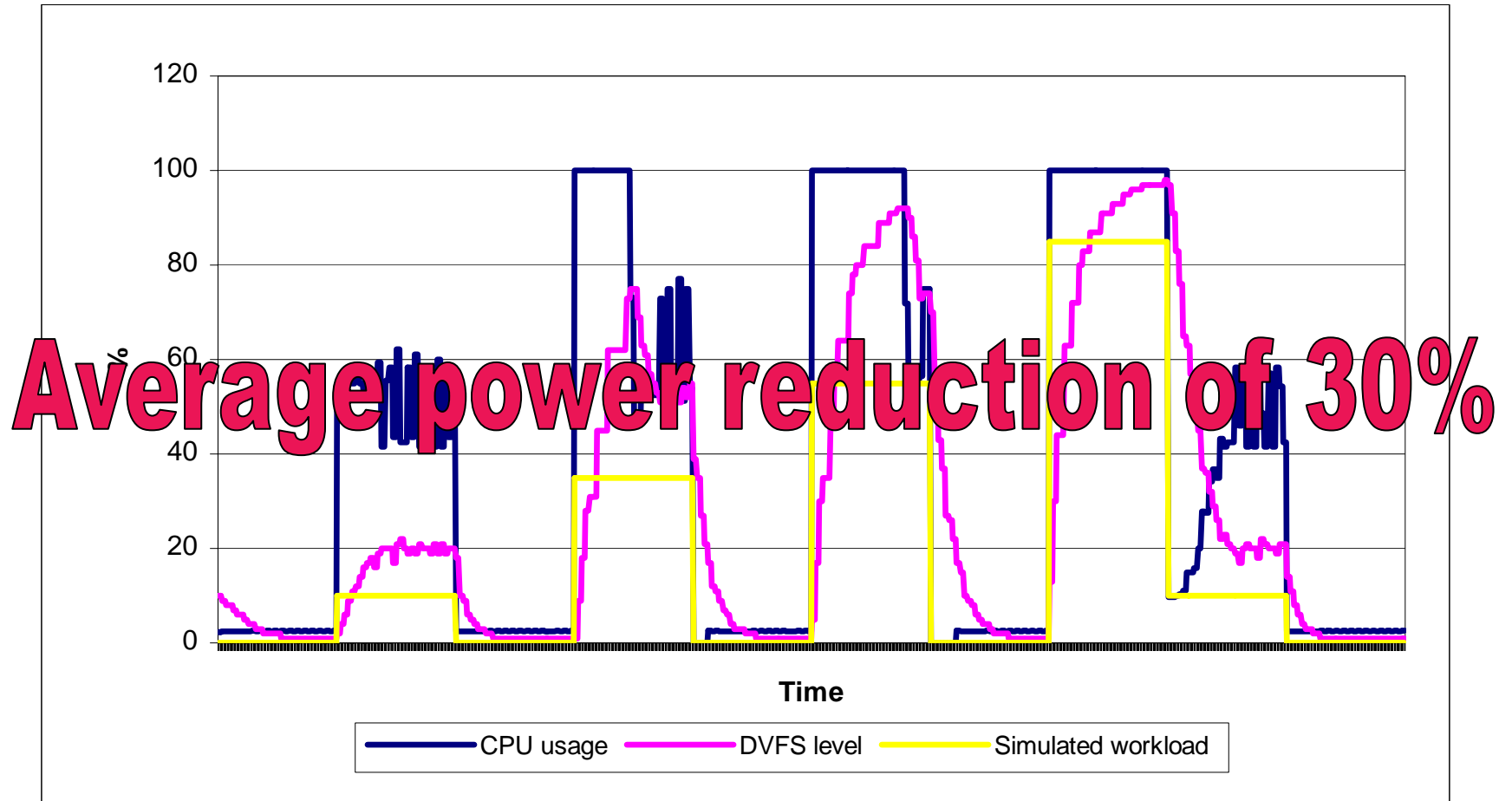
Main facts:  
0.065um  
Taped-out in 2005  
Linux-based system



# eChip Power Management Architecture



# eChip: Example of MPEG4 operations



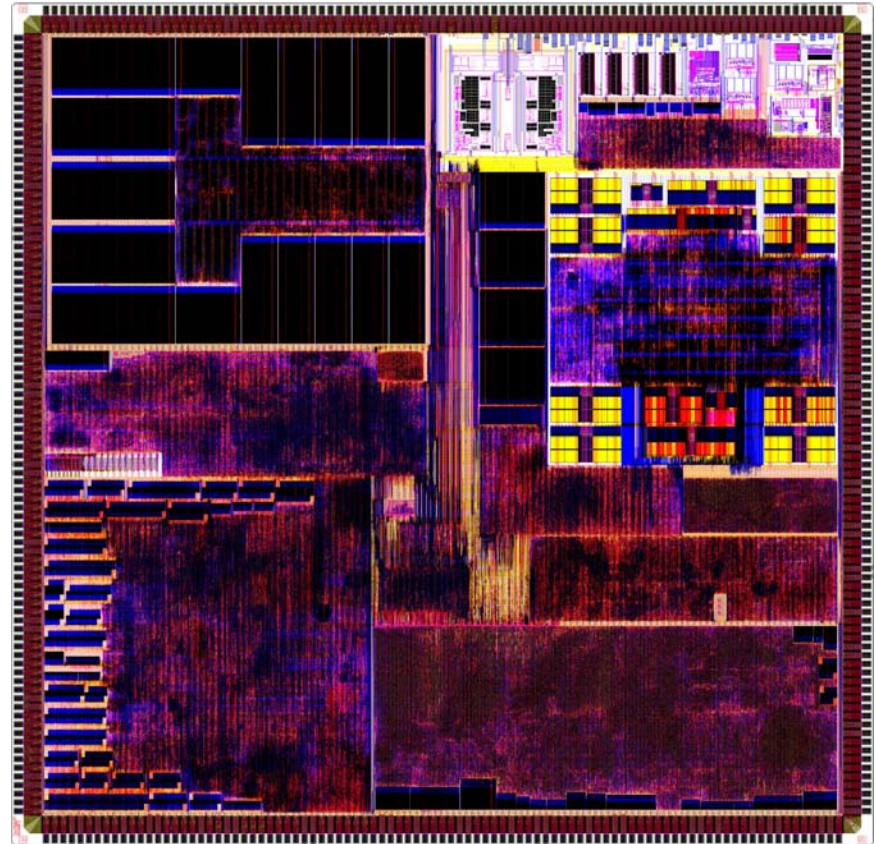




# Designing low-power products

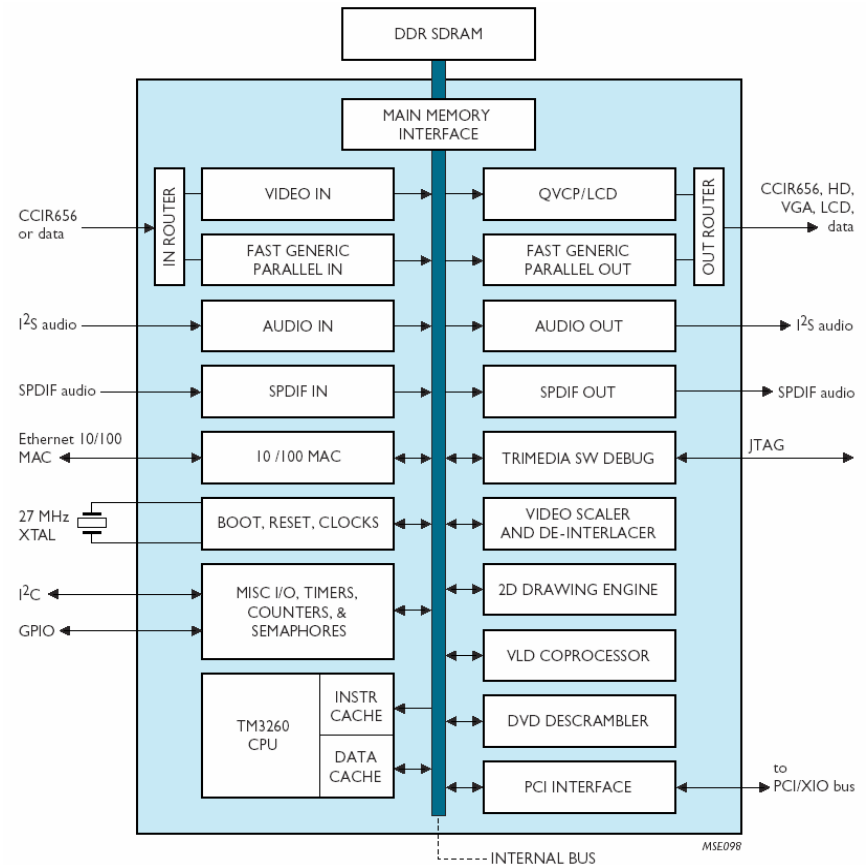
# Implementation Example

- **6.8M Gates + Analogue**
  - Including memories and macros
- **Aggressive die-size target**
  - 43mm<sup>2</sup> in 90nm
- **110/220 MHz target speed**
- **Low power**
  - Dynamic and Leakage
- **Multiple 3<sup>rd</sup> Party IP**
  - Including different graphics IP
- **Reduced power consumption up to 35%**



# Implementation Example 2

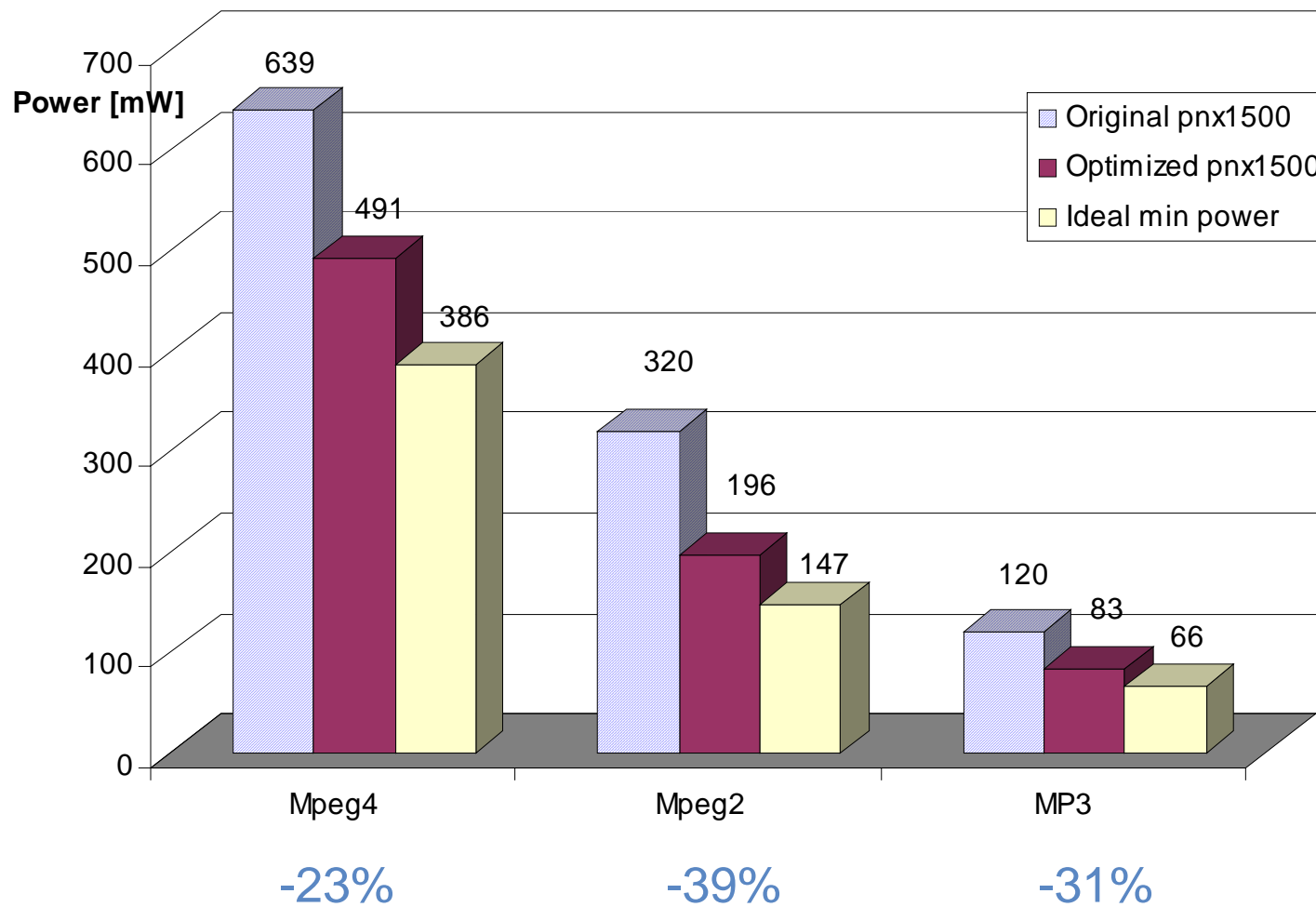
- ▶ This Media Processor is a complete Audio/Video/Graphics system on a chip capable of high quality software video, audio signal processing, as well as general purpose control processing.
- ▶ The architecture is memory centric, as every data communication occurs through writes and reads to background memory. The SoC is therefore build around the central data bus, the main memory interface, and the background memory.



# Implementation Example 2

- ▶ Original design based on fixed supply voltages but suited for voltage/frequency scaling.
- ▶ Optimisation step includes:
  - Partitioning in voltage domains
  - Closed-loop voltage/frequency scaling based on on-chip activity monitors and off-chip voltage regulators
  - Closed-loop process spread control.
  - Adaptive Back Biasing.
- ▶ As reference: “ideal case” assumed when we can scale voltage/frequency irrespective of the use cases.

# Implementation Example 2





# Conclusions

# Power is a pervasive problem

- ▶ Power is a problem due to technology scaling coupled with an increasing integration of features on new products, which are expected to run as usual on our old batteries for the usual low cost.
- ▶ Designing for low power affects all parts of the product conception and design cycle. Design teams need experience in low-power design
- ▶ Cost of low-power need to be well explained and (maybe) accepted
- ▶ Low-power requires co-operation in the industry, nobody can do it alone!

**Thank you for your attention**



