## ISLPED 2008 Program

**Monday August 11, 2008**

### 08:30-08:45

**Welcome by General and Program Co-Chairs**

### 08:45-09:45

**Towards a Green Electronic World: A Collaborative Approach**

Jaswinder Ahuja (Cadence Design Systems, Inc.)

[J.N. Tata Auditorium]

### 09:45-10:00

**Break**

### 10:00-12:00

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| **Session 1.1.2: Variation Tolerant Circuits**  
Session Chair: Niraj Bindal (Intel)  
Session Co-Chair: Chris Kim (University of Minnesota)  
Correlation Verification between Transistor Variability Model with Body Biasing and Ring Oscillation Frequency in 90nm Subthreshold Circuits  
Hiroshi Fuketa, Masanori Hashimoto, Yukko Mitsuymaya, Takao Onoye (Osaka University and JST, CREST)  
**Optimal Technology Selection for Minimizing Energy and Variability in Low Voltage Applications**  
Mingqo Seok, Dennis Sylvester, David Blaauw (University of Michigan)  
**Post-Silicon Programmed Body-Biasing Platform Suppressing Device Variability in 45 nm CMOS Technology**  
Hiroaki Suzuki, Masanori Kurimoto, Tadao Yamanaka, Hidehiro Takata (Renesas Technology Corp.), Hiroshi Makino (Osaka Institute of Technology), Hirofumi Shinohara (Renesas Technology Corp.)  
**Enhancing Beneficial Jitter Using Phase-Shifted Clock Distribution**  
Dong Jiao, Jie Gu, Pulkit Jain, Chris Kim (University of Minnesota) |  
**Session 2.1.1: Power Optimization**  
Session Chair: Wolfgang Nebel (University of Oldenburg)  
Session Co-Chair: Nagarajan Ranganathan (University of South Florida)  
Dynamic Virtual Ground Voltage Estimation for Power Gating  
Hao Xu, Ranga Vemuri, Wen-Ben Jone (University of Cincinnati)  
**A Mathematical Solution to Power Optimal Pipeline Design by Utilizing Soft Edge Flip-Flops**  
Mohammad Ghasemazar, Behnam Amelifar, Massoud Pedram (University of Southern California)  
**SRAM Methodology for Yield and Power Efficiency: Per-Element Selectable Supplies and Memory Reconfiguration Schemes**  
Rouwaida Kanj (IBM Austin Research Laboratories), Rajiv V. Joshi (IBM T.J. Watson Laboratories), Zhou Li, JB Kuang, Hung Ngo (IBM Austin Research Laboratories), Ying Zhou, Weiping Shi (Texas A&M University), Sani Nassif (IBM Austin Research Laboratories)  
**Reducing Wakeup Latency and Energy of MTCMOS Circuits via Keeper Insertion**  
Charbel J. Akl, Magdy A. Bayoumi (University of Louisiana at Lafayette)  
**Low-Power High-Accuracy Timing Systems for Efficient Duty Cycling**  
Thomas Schridl, Jonathan Friedman, Zainul Charbawala, Young H. Cho, Mani B. Srivastava (University of California, Los Angeles) |  
**A Parallel and Randomized Algorithm for Large-Scale Discrete Dual-Vt Assignment and Continuous Gate Sizing**  
Tai-Hsuan Wu, Lin Xie, Azadeh Davoodi (University of Wisconsin)  
**Multiple Power-Gating Domain (Multi-VGND) Architecture For Improved Leakage Power Reduction**  
Ashoka Sathanur (Politecnico di Torino), Luca Benini (Università di Bologna), Alberto Macii, Enrico Macii, Massimo Poncino (Politecnico di Torino) |

### 12:00-13:00

Lunch

### 13:00-15:00

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| **Session 1.1.3: Power Delivery and Timing**  
Session Chair: Swarup Bhunia (Case Western RU)  
Session Co-Chair: Radu Zlatanovici (Cadence Berkeley Labs)  
A Multi-Story Power Delivery Technique for 3D Integrated Circuits  
Pulkit Jain, Tae-Hyoun Kim, John Keane, Chris H. Kim (University of Minnesota)  
Energy Harvesting Photodiodes with Integrated 2D Diffractive Storage Capacitance  
Nathaniel J. Guilar, Erin G. Fong, Travis Keeburg, Diego R. Yankelevich, Rajeevan Amirtharajah (University of California, Davis)  
**SRAM Methodology for Yield and Power Efficiency: Per-Element Selectable Supplies and Memory Reconfiguration Schemes**  
Rouwaida Kanj (IBM Austin Research Laboratories), Rajiv V. Joshi (IBM T.J. Watson Laboratories), Zhou Li, JB Kuang, Hung Ngo (IBM Austin Research Laboratories), Ying Zhou, Weiping Shi (Texas A&M University), Sani Nassif (IBM Austin Research Laboratories)  
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**Session 2.1.2: Variability-Aware Optimization**  
Session Chair: Bharadwaj Amrutur (IISC)  
Session Co-Chair: Vishwani Agarwal (Auburn University)  
An Expected-Utility Based Approach to Variation Aware VLSI Optimization Under Scarce Information  
Upavan Gupta, Nagarajan Ranganathan (University of South Florida)  
**Reliability-centric Gate Sizing with Simultaneous Optimization of Soft Error Rate, Delay and Power**  
Koustav Bhattacharya, Nagarajan Ranganathan (University of South Florida)  
**Row/Column Redundancy to Reduce SRAM Leakage in Presence of Random Within-Die Delay Variation**  
Maziar Goudarzi, Tohru Ishihara (Kyushu University)  
**SRAM Methodology for Yield and Power Efficiency: Per-Element Selectable Supplies and Memory Reconfiguration Schemes**  
Rouwaida Kanj (IBM Austin Research Laboratories), Rajiv V. Joshi (IBM T.J. Watson Laboratories), Zhou Li, JB Kuang, Hung Ngo (IBM Austin Research Laboratories), Ying Zhou, Weiping Shi (Texas A&M University), Sani Nassif (IBM Austin Research Laboratories)  
**Low-Power High-Accuracy Timing Systems for Efficient Duty Cycling**  
Thomas Schridl, Jonathan Friedman, Zainul Charbawala, Young H. Cho, Mani B. Srivastava (University of California, Los Angeles) |
Variation-Aware Gate Sizing and Clustering for Post-Silicon Optimized Circuits
Cheng Zhuo, David Blaauw, Dennis Sylvester (University of Michigan)

Session 1.1.1: Low Voltage Logic and Memory
Session Chair: Hiroaki Suzuki (Renesas)
Session Co-Chair: Matt Ziegler (IBM)

Error-Resilient Low-Power Viterbi Decoders
Rami A. Abdallah, Naresh R. Shanbhag (University of Illinois at Urbana Champaign)

Increasing Minimum Operating Voltage (VDDmin) with Number of CMOS Logic Gates and Experimental Verification with up to 1Mega Stage Ring Oscillators
Taro Niiyama, Zhe Piao, Koichi Ishida (University of Tokyo), Masami Murakata (STARC), Makoto Takamiya, Takayasu Sakurai (University of Tokyo)

Thermal Analysis of 8-T SRAM for Nano-Scaled Technologies
Mesut Meteelliyo, Jaydeep P. Kulkarni, Kaushik Roy (Purdue University)

Analyzing Static and Dynamic Write Margin for Nanometer SRAMs
Jiajing Wang, Satyanand Nalam, Benton H. Calhoun (University of Virginia)

Panel: Penalty For Power Reduction - Performance or Schedule or Yield?
Bodhisatya Sarker (Cadence Design Systems (I) Pvt Ltd)
Nicco Bhabu (Cadence Design Systems (I) Pvt Ltd)
Arijit Dutta (Freescale Semiconductors)
Srinath D. (Kawasaki Micro)
Kaip Sridhar (Marvel Technologies)
Radhakrishnan Nair (SanDisk India)
Jayant Lahiri (ARM India)

Tuesday August 12, 2008
Design of Dual Threshold Voltages
Asynchronous Circuits
Behnam Ghavami, Hossein Pedram (Amirkabir University of Technology)

A low-power CMOS code-modulated multi-purpose dual-antenna receiver front-end
F. Tzeng, A. Jahanian, D. Pi, P. Heydari (University of California, Irvine)

O2C: Occasional Two-Cycle Operations for Dynamic Thermal Management in High Performance In-Order Microprocessors
Swaroop Ghosh, Jung-Hwan Choi, Patrick Ntai, Kauashik Roy (Purdue University)

A 150mV, process variation tolerant Schmitt trigger based sub-threshold SRAM
J. P. Kulkami, K. Roy (Purdue University)

Low Power High Bandwidth Amplifier with RC Miller and Gain Enhanced Feedforward Compensation
Shagun Bajoria, Vineet Kumar Singh, Raju Kunde, Chetan D. Parikh (Dhirubhai Ambani Institute of Information and Communication Technology)

Energy metering for free: augmenting switching regulators for real-time monitoring
P. Dutta (UC Berkeley), M. Feldmeier (MIT), J. Taneja (UC Berkeley), J. Paradiso (MIT), D. Culler (UC Berkeley)

Single Stage Static Level Shifter Design for Subthreshold to I/O Voltage Conversion
Yi-Shiang Lin, Dennis M. Sylvester (University of Michigan)

Power Reduction in On-Chip Interconnection Network by Serialization
Madan Arvind, Bharadwaj Amrutur (Indian Institute of Science)

A Probabilistic Technique for Full-chip Leakage Estimation
Shaobo Lu, Qinru Oiu, Qing Wu (Binghamton University, State University of New York)

Bus Encoding for Simultaneous Delay and Energy Optimization
Jingyi Zhang, Qing Wu, Qinru Oiu (Binghamton University, State University of New York)

Frequency Planning for Multi-Core Processors Under Thermal Constraints
Michael Kadin, Sherief Reda (Brown University)

Reducing Leakage Power by Accounting for Temperature Inversion Dependence in Dual-Vt Synthesized Circuits
Andrea Calimeri (Politecnico di Torino), R. Iris Bahar (Brown University), Enrico Macii, Massimo Poncino (Politecnico di Torino)

Variability of Flip-Flop Timing at Sub-Threshold Voltages
Niklas Lotze, Maurits Ortmanns, Yiannos Manoli (University of Freiburg)

Low Power Current Mode Receiver With Inductive Input Impedance
Marshnil V. Dave, Maryam Shojaei Baghini, Dinesh Sharma (Indian Institute of Technology, Bombay)

Analytical Results for Design Space Exploration of Multi-core Processors Employing Thread Migration
Ravishankar Rao, Samir Vrudhula, Krzysztof Berezowski (Arizona State University)

A Physical Level Study and Optimization of CAM-Based Checkpointed Register Alias Table
Elham Safi, Andreas Moshovos, Andreas Veneris (University of Toronto)

Enhancing Energy Efficiency of Processor-Based Embedded Systems through Post-Fabrication ISA Extension
Hamid Noori (Institute of Systems, Information Technologies and Nanotechnologies), Farhad Mehdipour, Koji Inoue, Kazuaki Murakami (Kyushu University)

Optimal Power and Noise Allocation for Analog and Digital Sections of a Low Power Radio Receiver
Kannan Aryaperumal Sankaragomathi, Manodipan Sahoo, Satyam Dwivedi, Bharadwaj S. Amrutur, Navakanta Bhat (Indian Institute of Science)

Tutorial: A Tutorial on Test Power
Vishwani D. Agrawal (Auburn University)
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<td>Industry Session</td>
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<td>Session Chair: Rabi N. Mahapatra (Texas A&amp;M University)</td>
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<td>Session Co-Chair: Massimo Poncino (Politecnico di Torino)</td>
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<td>SOC Designs in the Energy Conscious Era</td>
<td>Simultaneous Optimization of Battery-Aware Voltage Regulator Scheduling with Dynamic Voltage and Frequency Scaling</td>
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<td>Srirkanth Jadhcha (Synopsys Inc.)</td>
<td>Youngjin Cho, Younghun Kim, Yongsoo Joo, Kyungsuo Lee, Naehyuck Chang (Seoul National University)</td>
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<td>Expected System Energy Consumption</td>
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<td>Tutorial: Clock Gating for Power Optimization in ASIC Design Cycle: Theory &amp; Practice</td>
<td>Hybrid Dynamic Thermal Management Based on Statistical Characteristics of Multimedia Applications</td>
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<td>Jairam S, Madhusudan Rao, Jithendra Srinivas, Parimala Vishwanath, Udayakumar H., Jagdish Rao (Texas Instruments)</td>
<td>Inchoon Yeo, Eun Jung Kim (Texas A&amp;M University)</td>
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<td>09:30-09:45</td>
<td>Break</td>
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<td>09:45-10:45</td>
<td>Advances in Low Power Verification</td>
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<td>Janick Bergeron (Synopsys, Inc.)</td>
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<td>10:45-12:15</td>
<td>Tutorial: Low Power Chips: A Fabless ASIC Perspective</td>
<td>Session 2.2.1: System-Level Power Estimation</td>
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<td>Shashank Bhone (Open-Silicon Research Pvt Ltd), Vamsi Boppana (Open-Silicon, Inc.)</td>
<td>Session Chair: Todd Austin (University of Michigan)</td>
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<td>Session Co-Chair: Naehyuck Chang (Seoul National University)</td>
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<td>A Framework for Energy Consumption Based Design Space Exploration for Wireless Sensor Nodes</td>
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<td>Sonali Chouhan, M. Balakrishnan, Ranjan Bose (Indian Institute of Technology Delhi)</td>
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<td>Full-System Chip Multiprocessor Power Evaluations Using FPGA-Based Emulation</td>
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<td>Ablishek Bhattacharjee, Gilberto Contreras, Margaret Martonosi (Princeton University)</td>
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<td>Noninvasive Leakage Power Tomography of Integrated Circuits by Compressive Sensing</td>
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<td>Davood Shamsi, Petros Boufounos, Farinaz Koushanfar (Rice University)</td>
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## Session 1.2.2: Microarchitectural Techniques

**Session Chair:** Masaaki Kondo (University of Tokyo)  
**Session Co-Chair:** Koji Inoue (Kyushu University)

### Impact of Dynamic Voltage and Frequency Scaling on the Architectural Vulnerability of GALS Architectures
Niranjan Soundararajan, Vijaykrishnan Narayanan, Anand Sivasubramaniam (The Pennsylvania State University)

### Instruction-Driven Clock Scheduling with Glitch Mitigation
Gu-Yeon Wei, David Brooks, Ali Durlov Khan, Xiaoyao Liang (Harvard University)

### Thread Fusion
José González, Qiong Cai, Pedro Chaparro, Grigorios Magklis (UPC-Intel Lab Barcelona), Ryan Rakvic (United States Naval Academy, Annapolis), Antonio González (UPC-Intel Lab Barcelona)

### Power-Efficient Clustering via Incomplete Bypassing
Eric P. Villasenor, DaeHo Seo, Mithuna S. Thottethodi (Purdue University)

### Lazy Instruction Scheduling: Keeping Performance, Reducing Power
Ali Mahjur (Shahid Beheshti University), Mahmud Taghizadeh, Amir Hossein Jahangir (Sharif University of Technology)

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15:15-15:30  
**Break**

15:30-16:30  
**On the Rules of Low-Power Design (and How to Break Them)**  
Todd M. Austin (University of Michigan)  
[J.N. Tata Auditorium]

16:30-17:30  
**Next-Generation Power-Aware Design**  
Takayasu Sakurai (The University of Tokyo)  
[J.N. Tata Auditorium]

17:30  
**Closing Remarks**  
[J.N. Tata Auditorium]