2010 International Symposium on Low Power Electronics and Design (ISLPED)

Omni Hotel, Downtown Austin, TX, USA
August 18-20, 2010

http://www.islped.org/

Wednesday, August 18, 2010		
08:00-08:30	**Continental Breakfast - Foyer**	
08:30-08:45	**Welcome by General and Program Co-Chairs** General Chairs: Vojin Oklobdzija, Univ. of Texas, Dallas and Barry Pangle, Mentor Graphics General Vice-Chair: Naehyuck Chang, Seoul National Univ. Program Chairs: Chris Kim, Univ. of Minnesota, and Naresh Shanbhag, Univ. of Illinois at Urbana-Champaign	
08:45-09:30	**Keynote Talk 1 – Capital Ballroom** Chair: Naresh Shanbhag, Univ. of Illinois at Urbana-Champaign	
	Jan Rabaey, UC Berkeley Going Beyond Turing: Energy-efficiency in the Post-Moore Era	
09:30-10:15	**Keynote Talk 2 – Capital Ballroom** Chair: Barry Pangle, Mentor Graphics	
	Raj Jammy, VP, Materials and Emerging Technologies, SEMATECH Emerging Low Power Technologies: CMOS or Beyond CMOS?	
10:15-10:30	**Break - Foyer**	
10:30-12:30	**1.1.1. Alternative Memory and Emerging Devices (Capital Ballroom A)** Chair: Mike Clinton, Texas Instruments Co-chair: Rahul Rao, IBM *This session highlights emerging technologies and their application to memory and logic design. These technologies include embedded DRAMs, spin-torque-transfer RAMs, memristors and nano-electromechanical switches. The papers present analysis and approaches for improving sense margins, thermal sensitivity, variation tolerance and energy of operation.*	**2.2.1. Variation-aware and Reconfigurable Design (Capital Ballroom B)** Chair: Sani Nassif, IBM Co-chair: Naehyuck Chang, Seoul National Univ. *This session covers process variation and power issues. The first three papers focus on the process variation issues, targeting mainstream CMOS circuit, low-power sub-threshold circuit, and emerging silicon photonic interconnects. The last two papers focus on power and thermal related design issues of reconfigurable architecture and circuit.*
	[BEST PAPER CANDIDATE] **Combined Magnetic- and Circuit-level Enhancements for the Nondestructive Self-Reference Scheme of STT-RAM** Yiran Chen, *Hai Li, Xiaobin Wang, Wenzhong Zhu, **Wei Xu, **Tong Zhang *Seagate Technology* **Polytechnic Institute of NYU* ***Rensselaer Polytechnic Institute*	**[BEST PAPER CANDIDATE]** **Power-Efficient Variation-Aware Photonic On-Chip Network Management** Moustafa Mohamed, Zheng Li, Xi Chen, Li Shang, Alan Mickelson, Manish Vachharajani, *Yihe Sun *Univ. of Colorado at Boulder* **Tsinghua National Laboratory for Information Science and Technology*

	A New Paradigm in the Design of Energy-Efficient Digital Circuits Using Laterally-Actuated Double-Gate NEMS Hamed Dadgour, Kaustav Banerjee *UCSB*	**VAIL: Variation-Aware Issue Logic and Performance Binning for Processor Yield and Profit Improvement** Somnath Paul, Swarup Bhunia *Case Western Reserve Univ.*
	Analysis of Thermal Behaviors of Spin-Torque-Transfer RAM: A Simulation Study [short] Subho Chatterjee, *Sayeef Salahuddin, Satish Kumar, Saibal Mukhopadyay *Georgia Tech* **UC Berkeley*	**Low-Power Sub-threshold Design of Secure Physical Unclonable Functions** [short] Lang Lin, *Dan Holcomb, Dilip Kumar Krishnappa, Prasad Shabadi, Wayne Burleson *Univ. of Massachusetts Amherst* **Univ. of California Berkeley*
	Variation Aware Performance Analysis of Gain Cell Embedded DRAMs [short] Wei Zhang, Ki Chul Chun, Chris H. Kim *Univ, of Minnesota*	**Exploiting Power Budgeting in Thermal-Aware Dynamic Placement for Reconfigurable Systems** [short] Shahin Golshan, Eli Bozorgzadeh, *Benjamin Schafer, *Kazutoshi Wakabayashi, Houman Homayoun, Alex Veidenbaum, *UCI* **NEC Corp. Central Research Laboratories*
	Low-power Dual-element Memristor-Based Memory Design [short] Dimin Niu, *Yiran Chen, Yuan Xie *Penn State Univ.* **Seagate Technology*	**3D-NonFAR: Three-Dimensional Non-Volatile FPGA Architecture Using Phase Change Memory** [short] Yibo Chen, Jishen Zhao, Yuan Xie *Penn State Univ.*
12:30-13:30	**Lunch – Atrium Lobby**	
13:30-15:30	**1.2.1. Microarchitectures and Scheduling (Capital Ballroom A)** Chair: Amy Novak, AMD Co-chair: Eren Kursun, IBM *This session addresses novel microarchitectures to optimize the power consumption of on-chip networks and application specific systems. The last paper of this session presents a scheduling technique for thermal and power management.*	**1.3.1. Low-Power Design for Scaled Low-Voltage Processes (Capital Ballroom B)** Chair: Gary Carpenter, IBM Co-chair: Atila Alvandpour, Linköping Univ. *This session highlights advances in the design of a variety of low-power circuits for scaled, low-voltage processes and applications.*
	Low-Power Current-Mode Transceiver for On-chip Bidirectional Buses Marshnil Dave, Rajkumar Satkuri, Mahavir Jain, Maryam Shojaei, Dinesh Sharma *IIT-Bombay*	**[BEST PAPER CANDIDATE]** **A 6μW, 100Kbps, 3-5GHz, UWB Impulse Radio Transmitter** Rajeev Dokania, Xiao Wang, Carlos Dorta-Quinones, Wacek Godycki, Siddharth Tallur, Alyssa Apsel *Cornell Univ.*
	Low Power Branch Prediction for Embedded Application Processors [short] Nadav Levison, Shlomo Weiss *Tel Aviv Univ.*	**A 65nm CMOS Low-Power, Low-Voltage Bandgap Reference with Using Self-biased Composite Cascode Opamp** Leila Koushaeian, Stan Skafidas *Victoria Univ., Melbourne, Australia*

	Reducing Variability in Chip-Multiprocessors with Adaptive Body Biasing [short] Alyssa Bonnoit, Lawrence Pileggi *Carnegie Mellon Univ.*	**A 5V Output Voltage Boost Switching Converter with Hybrid Digital and Analog PWM Control** Chien-Chun Lu, Ming-Ching Kuo *ITRI*
	Diet SODA: A Power-Efficient Processor for Digital Cameras [short] Sangwon Seo, Ronald Dreslinski, Mark Woh, Scott Mahlke, Trevor Mudge, *Chaitali Chakrabarti *Univ. of Michigan* **Arizona State Univ.*	**A Low-Power Digitally-Programmable Variable Gain Amplifier in 65 nm CMOS** Amir Zjajo, *Mingxin Song *Delft Univ. of Technology* **Harbin Univ. of Science and Tech.*
	Temperature- and Energy-Constrained Scheduling in Multitasking Systems: A Model Checking Approach [short] Weixun Wang, Xiaoke Qin, Prabhat Mishra *Univ. of Florida*	
15:30-15:45	**Break -Foyer**	
15:45-17:15	**Poster Session – Balcony** Chair: Manish Goel, Texas Instruments	
	P1. PEEC Based Parasitic Modeling for Power Analysis on Custom Rotary Rings Vinayak Honkote, Baris Taskin *Drexel Univ.*	**P2. HERQULES: SYSTEM LEVEL CROSS-LAYER DESIGN EXPLORATION FOR EFFICIENT ENERGY-QUALITY TRADE-OFFS** Georgios Karakonstantis, Georgios Panagopoulos, Kaushik Roy *Purdue Univ.*
	P3. Analog Circuit Shielding Routing Algorithm Based on Net Classification Qiang Gao, Yin Shen, Yici, Cai, Hailong Yao *Tsinghua Univ.*	**P4. MODEST : A Model for Energy Estimation under Spatio-Temporal Variability** Shrikanth Ganapathy, Ramon Canal, Antonio Gonzalez, Antonio Rubio *Universitat Politecnica de Catalunya*
	P5. Replication-Aware Leakage Management in Chip Multiprocessors with Private L2 Caches Hyunhee Kim, Jihong Kim, Jung Ho Ahn *Seoul National Univ.*	**P6. Exploring Custom Instruction Synthesis for Application-Specific Instruction Set Processors with Multiple Design Objectives** Hai Lin, Yunsi Fei *Univ. of Connecticut*
	P7. Energy Efficient Implementation of Parallel CMOS Multipliers with Improved Compressors Dursun Baran, Mustafa Aktan, Vojin G. Oklobdzija *Univ. of Texas at Dallas*	**P8. RealEnergy: a New Framework and a Case Study to Evaluate Power-Aware Real-Time Scheduling Algorithms** Jian Lin, Albert Cheng, Wei Song *Univ. of Houston*
	P9. A Low-Power Clock Gating Cell Optimized for Low-Voltage Operation in a 45-mn Technology Martin Saint-Laurent, Animesh Datta *Qualcomm*	**P10. Dynamic Thermal Management for Single and Multicore Processors Under Soft Thermal Constraints** Bing Shi, Yufu Zhang, Ankur Srivastava *Univ. of Maryland, College Park*

	P11. A Three-Phase Power-Gating Turn-on Technique for Controlling Ground Bounce Noise Rahul Singh, Ah-Reum Kim, *SoYoung Kim, Suhwan Kim *Seoul National Univ.* **Sungkyunkwan Univ.*	**P12. Customizing Pattern Set for Test Power Reduction via Improved X-identification and Reordering** Krishna Kumar S, S. Kaundinya, Subhadip Kundu, Santanu Chattopadhyay *Indian Institute of Tech. Kharagpur*
	P13. Analysis and Design of Ultra Low Power Thermoelectric Energy Harvesting Systems Chao Lu, Sang Phill Park, Vijay Raghunathan, Kaushik Roy *Purdue Univ.*	**P14. RAPL: Memory Power Estimation and Capping** Howard David, Eugene Gorbatov, Ulf Hanebutte, Rahul Khanna, Christian Le *Intel*
	P15. Energy Efficient Proactive Thermal Management in Memory Subsystem Raid Ayoub, Krishnam Indukuri, Tajana Rosing *UCSD*	**P16. Power-performance Management on an IBM POWER7 Server** Karthick Rajamani, Freeman Rawson, Malcolm Ware, Heather Hanson, John Carter, Todd Rosedahl, Andrew Geissler, Guillermo Silva, Hong Hua *IBM*
	P17. Energy and Thermal-Aware Video Coding via Encoder/Decoder Workload Balancing Domenic Forte, Ankur Srivastava *Univ. of Maryland*	**P18. Tradeoff between Energy Savings and Privacy Protection in Computation Offloading** Jibang Liu, Karthik Kumar, Yung-Hsiang Lu *Purdue Univ.*
	P19. 0.5-V Operation Variation-Aware Word-Enhancing Cache Architecture Using 7T/14T hybrid SRAM Yohei Nakata, Shunsuke Okumura, Hiroshi Kawaguchi, Masahiko Yoshimoto *Kobe Univ.*	**P20. Workload-Adaptive Process Tuning Strategy for Power-Efficient Multi-Core Processors** Jungseob Lee, *Chi-Chao Wang, Hamid Gashemi, **Lloyd Bircher, *Yu Cao, Nam Sung Kim *Univ. of Wisconsin-Madison* **Arizona State Univ.* ***Advanced Micro Devices*
	P21. Small-Area and Low-Energy K-Best MIMO Detector Using Relaxed Tree Expansion and Early Forwarding Tae-Hwan Kim, In-Cheol Park *KAIST*	
17:30-19:00	**Wine and Cheese Reception - Foyer**	

Thursday, August 19, 2010	
08:00-08:30	**Continental Breakfast – Foyer**
08:30-09:15	**Keynote Talk 3 – Capital Ballroom** Chair: Chris H. Kim, Univ. of Minnesota
	Ajith Amerasekera, Kilby Research Labs, Texas Instruments Inc., Dallas, TX Ultra Low Power Electronics in the Next Decade
09:15-10:00	**Keynote Talk 4 – Capital Ballroom** Chair: Vojin Oklobdzija, Univ. of Texas, Dallas
	Kevin Nowka, Sr. Manager VLSI Systems Research, IBM Research-Austin Technology variability and uncertainty implications for power efficient VLSI systems

10:00-10:15	**Break -Foyer**	
10:15-12:15	**1.1.2. Voltage Scaling and Adaptation for Low-Power (Capital Ballroom A)** Chair: Keith Bowman, Intel Co-chair: Srini Sridhara, TI *The session highlights voltage scaling and adaptation for reducing power consumption. The topics covered include voltage scaling based on processor workload, NBTI degradation, and on-chip power measurement. Papers in the session also address operational time adaptation to reduce leakage and clock network design for ultra-low voltage systems.*	**2.3.1. Analysis and Optimization for Energy-efficient Systems (Capital Ballroom B)** Chair: Thomas Wenisch, Univ. of Michigan Co-chair: Vivek Tiwari, Intel *This session presents analysis and optimization techniques across a wide range of energy-aware applications. Two of the applications are for automobiles - batteries for hybrids and electronic control. Other applications include antenna design for mobile devices, heterogeneous storage systems and a bio-medical application for seizure detection.*
	Workload-Aware Neuromorphic Design of Low-Power Supply Voltage Controller [short] Saurabh Sinha, Jounghyuk Suh, Bertan Bakkaloglu, Yu Cao *Arizona State Univ.*	**[BEST PAPER CANDIDATE]** **Large-Scale Battery System Modeling and Analysis for Emerging Electric-Drive Vehicles** Kun Li, Jie Wu, Yifei Jiang, Zyad Hassan, Qin Lv, Li Shang, Dragan Maksimovic *Univ. of Colorado*
	Distributed DVFS Using Rationally-Related Frequencies and Discrete Voltage Levels [short] Jean-Michel Chabloz, Ahmed Hemani *KTH Stockholm*	**Power-Efficient Directional Wireless Communication on Small Form-Factor Mobile Devices** Ardalan Amiri Sani, Hasan Dumanli, Lin Zhong, Ashutosh Sabharwal *Rice Univ.*
	NBTI-Aware DVFS: A New Approach to Saving Energy and Increasing Processor Lifetime [short] Mehmet Basoglu, Mattan Erez, Michael Orshansky *Univ. of Texas at Austin*	**Dynamic Thermal Management for Networked Embedded Systems under Harsh Ambient Temperature Variation** [short] Sangyoung Park, *Jian-Jia Chen, Donghwa Shin, Younghyun Kim, **Chia-Lin Yang, Naehyuck Chang, *Seoul National Univ.* **ETH Zurich* ***National Taiwan Univ.*
	In-Situ Power Monitoring Scheme and Its Application in Dynamic Voltage and Threshold Scaling for Digital CMOS Integrated Circuits [short] Nandish Mehta, Gururaj Naik, Bharadwaj Amrutur *Indian Institute of Science*	**PS-BC: Power-saving Considerations in Design of Buffer Caches Serving Heterogeneous Storage Devices** [short] Feng Chen and Xiaodong Zhang *Ohio State Univ.*
	Leakage Minimization Using Self Sensing and Thermal Management [short] Alireza Vahdatpour, Modrag Potkonjak *UCLA*	**Low-Power DWT-Based Quasi-Averaging Algorithm and Architecture for Epileptic Seizure Detection** [short] Himanshu Markandeya, Georgios Karakonstantis, Shriram Raghunathan, Pedro Irazoqui, Kaushik Roy *Purdue Univ.*
	Clock Network Design for Ultra-Low Power Applications [short] Mingoo Seok, David Blaauw, Dennis Sylvester *Univ. of Michigan*	
12:15-13:15	**Lunch – Atrium Lobby**	

<table>
<tr><td>13:15-
14:45</td><td>2.2.2. Energy Harvesting and Power Conversion Systems (Capital Ballroom A)

Chair: Vijay Raghunathan, Purdue Univ.

This session addresses several important topics in energy harvesting and power conversion systems. The first two papers cover maximum power transfer or maximum power point tracking in supercapacitor-based energy systems. The third paper models the peak power consumption for data center servers considering the power supply dynamics, and the last paper deals with energy-efficient task scheduling in real-time energy-harvesting embedded systems.</td><td>2.1.1. Thermal, Variability, and Reliability Considerations in Power-Aware Design (Capital Ballroom B)

Chair: Feng Shi, Yale Univ.
Co-chair: Azadeh Davoodi, Univ of Wisconsin Madison

In this session, new methods are discussed to characterize and optimize power from thermal, variability, and reliability point of view. The first paper proposes spatial characterization of power based on thermal infrared emissions. The second paper evaluates various methods of statistical estimation of leakage power. The last paper proposes a dynamic cache indexing method to explore power gating in order to minimize the aging effects.</td></tr>
<tr><td></td><td>Maximum Power Transfer Tracking for a Photovoltaic-Supercapacitor Energy System [short]

Younghyun Kim, Naehyuck Chang, *Yanzhi Wang, *Massoud Pedram,

Seoul National Univ.
*Univ. of Southern California</td><td>[BEST PAPER CANDIDATE]

Post-Silicon Power Characterization Using Thermal Infrared Emissions

Ryan Cochran, Abdullah Nowroz, Sherief Reda

Brown Univ.</td></tr>
<tr><td></td><td>DuraCap: a Supercapacitor-Based, Power-Bootstrapping, Maximum Power Point Tracking Energy-Harvesting System [short]

Chien-Ying Chen, *Pai Chou

National Tsing Hua Univ.
*UC Irvine</td><td>Statistical Leakage Modeling for Accurate Yield Analysis: The CDF Matching Method and Its Alternatives

Rouwaida Kanj, Rajiv Joshi, Sani Nassif

IBM</td></tr>
<tr><td></td><td>Peak Power Modeling for Data Center Servers with Switched-Mode Power Supplies [short]

David Meisner, Thomas Wenisch

Univ. of Michigan</td><td rowspan="2">Dynamic Indexing: Concurrent Leakage and Aging Optimization for Caches

Andrea Calimera, *Mirko Loghi, Enrico Macii, Massimo Poncino

Politecnico di Torino
*Universita' di Udine</td></tr>
<tr><td></td><td>Load-Matching Adaptive Task Scheduling for Energy Efficiency in Energy Harvesting Real-Time Embedded Systems [short]

Shaobo Liu, Jun Lu, Qing Wu, Qinru Qiu

State Univ. of New York at Binghamton</td></tr>
<tr><td>14:45-
15:00</td><td colspan="2">Break -Foyer</td></tr>
<tr><td>15:00-
16:30</td><td>Special Session 1- Energy-efficiency via Error-Resiliency (Capital Ballroom A)

Chair: Subhasish Mitra, Stanford Univ.</td><td>Special Session 2 - Energy Storage Systems for Emerging Applications (Capital Ballroom B)

Chair: Naehyuck Chang, Seoul National Univ.</td></tr>
<tr><td></td><td>Benjamin Vigoda, Lyric Semiconductor Inc
Low Power Logic for Statistical Signal Processing</td><td>Jeffrey Lee, LG
Battery and management technology for an extended-range electric vehicle</td></tr>
<tr><td></td><td>Keith Bowman, Intel Corporation, Hillsboro, OR
Resilient Microprocessor Design for High Performance & Energy Efficiency</td><td>Massoud Pedram, Univ. of Southern California
Hybrid electrical energy storage systems</td></tr>
<tr><td></td><td>Rakesh Kumar, Univ. of Illinois at Urbana-Champaign
Computing with Stochastic Processors: Revisiting the Correctness Contract between Software and Hardware</td><td>Kathryn Miles, EETrex
Vehicle to smart grid integration technologies challenges</td></tr>
<tr><td></td><td>Ravi Nair, IBM
Models for Energy-Efficient Approximate Computation</td><td>Li Shang, Univ. of Colorado, Boulder
Hybrid energy storage system integration for vehicles</td></tr>
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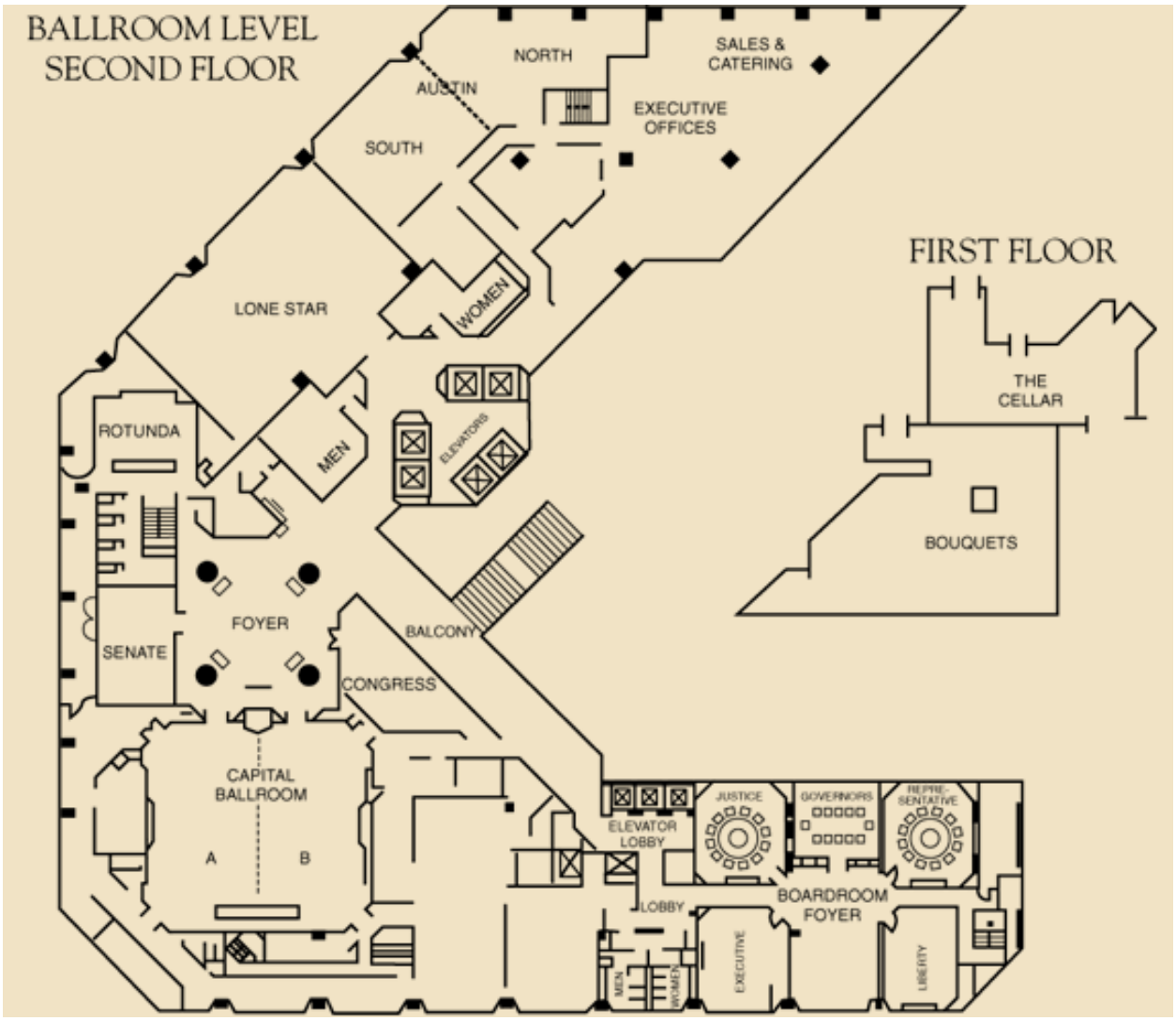
16:30-16:45	**Break -Foyer**	
16:45-17:45	**Special Session 3- Energy Efficient Smart Buildings (Capital Ballroom A)** Chair: Vijay Raghunathan, Purdue Univ.	**Embedded Tutorial (Capital Ballroom B)** Chair: Rahul Rao, IBM
	Mani Srivastava, UC Los Angeles Fine-grained Resource Monitoring in Residential Buildings	**Mondira Pant, Intel** Microprocessor Power Delivery Challenges in the Nanoscale Era
	Rajesh Gupta, UC San Diego Cyber-Physical Energy Systems	
18:30-	**Banquet – Mansion at Judge's Hill** http://www.mansionatjudgeshill.com/	

Friday, August 20, 2010

08:00-08:30	**Continental Breakfast - Foyer**	
08:30-10:00	**1.2.2. Memory System Design (Capital Ballroom A)** Chair: Jian Li, IBM Co-chair: Alper Buyuktosunoglu, IBM *This session discusses new technologies and microarchitectural techniques to achieve high energy efficiency in caches and other memory systems*	**2.1.2. Design Optimization for Low Power (Capital Ballroom B)** Chair: Sumit DasGupta, Silicon Integration Initiative (Si2) Co-chair: Vishwani D. Agrawal *The first paper discusses placement and routing methods targeting reduction of clock and leakage components of power. The second paper addresses dual-Vdd design of near-threshold design; optimizing global routing to reduce power consumption due to long wires is proposed in the third paper. The last paper proposes the synthesis of wakeup network of power gating circuits for fast wakeup.*
	TurboTag: Lookup Filtering to Reduce Coherence Directory Power Pejman Lotfi-Kamran, *Michael Ferdman, Daniel Crisan, Babak Falsafi *EPFL* **CMU/EPFL*	**PASAP: Power Aware Structured ASIC Placement** Ashutosh Chakraborty, David Pan *Univ. of Texas at Austin*
	Rank-Aware Cache Replacement and Write Buffering to Improve DRAM Energy Efficiency Ahmed Amin, *Zeshan Chishti *Purdue Univ.* **Intel*	**Automatic Synthesis of Near-Threshold Circuits with Fine-Grain Performance Tunability** [short] Mohammad Reza Kakoee, *Ashoka Sathanur, **Antonio Pullini, *Jos Huisken, Luca Benini *Università di Bologna* **IMEC Netherlands* ***EPFL*
	An Energy Efficient Cache Design Using Spin Torque Transfer (STT) RAM Mitchelle Rasquinha, Dhruv Choudhary, Subho Chatterjee, Saibal Mukhopadhyay, Sudhakar Yalamanachili *Georgia Institute of Technology*	**A Pareto-Algebraic Framework for Signal Power Optimization in Global Routing** [short] Hamid Shojaei, Tai-Hsuan Wu, Azadeh Davoodi, *Twan Basten *Univ. of Wisconsin-Madison* **Eindhoven Univ. of Technology*

		Wakeup Synthesis and Its Buffered Tree Construction for Power Gating Circuit Designs [short] Seungwhun Paik, Sangmin Kim, Youngsoo Shin *KAIST*
10:00-10:15	**Break -Foyer**	
10:15-11:45	**2.3.2. Power Analysis for High-Performance Microprocessor Design Techniques (Capital Ballroom A)** Chair: Steve Curtis, Intel Co-chair: Ron Preston, Intel *This session analyzes the power/performance characteristics of power optimization techniques for high performance microprocessors. These include dynamic power management for multi-processor SoCs; dynamic voltage and frequency scaling; and software based transaction memory.*	**Design Contest (Capital Ballroom B)** Chair: Vasily Moshnyaga, Fukuoka University *This session is devoted to the Low Power Design Contest. A panel of experts from industry and academia has selected 4 winning designs out of 14 submissions. Winners will present original power-aware designs and highlight innovations and design choices made for improving energy efficiency.*
	Accurate Modeling and Calculation of Delay and Energy Overheads of Dynamic Voltage Scaling in Modern High-Performance Microprocessors Jaehyun Park, Donghwa Shin, *Massoud Pedram, Naehyuck Chang *Seoul National Univ.* **Univ. of Southern California*	**Hijacking Power and Bandwidth from the Mobile Phone's Audio Interface** Ye-Sheng Kuo, Thomas Schmid and Prabal Dutta *University of Michigan*
	Custom Feedback Control: Enabling Truly Scalable On-Chip Power Management for MPSoCs [short] Siddharth Garg, Diana Marculescu, Radu Marculescu *Carnegie Mellon Univ.*	**A 20µW, 3-5GHz, FCC-Compliant, Dual-Band UWB Impulse Radio for Sensor networks** Rajeev Dokania, Xiao Wang, Siddharth Tallur, Carlos Dorta-Quinones, Waclaw Godycki and Alyssa Apsel *Cornell University*
	STM versus Lock-based Systems: An Energy Consumption Perspective [short] Felipe Klein, Alexandro Baldassin, Joao Moreira, Paulo Centoducatte, Sandro Rigo, Rodolfo Azevedo *UNICAMP*	**A 2µw AES Core with DPA Attack Countermeasure** Yibo Fan, Guoyu Qian, Satoshi Goto and *Yukiyasu TSUNOO *Waseda University* **NEC Corp.*
	Dynamic Workload Characterization for Power Efficient Scheduling on CMP Systems [short] Gaurav Dhiman, Vasileios Kontorinis, Dean Tullsen, Tajana Rosing, *Eric Saxe, *Jonathan Chew *UC San Diego* **Sun Microsystems*	**System-Level Low Power Design for Ultra High Definition H.264/AVC Video Decoder** Dajiang Zhou, Jinjia Zhou, Xun He, *Ji Kong, *Jiayi Zhu, *Peilin Liu and Satoshi Goto *Waseda University* **Shanghai Jiao Tong University*
11:45	**Closing of ISLPED 2010**	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