ISLPED 2025

INTERNATIONAL SYMPOSIUM ON LOW POWER ELECTRONICS AND DESIGN

August 6-8, 2025, University of Iceland, Iceland

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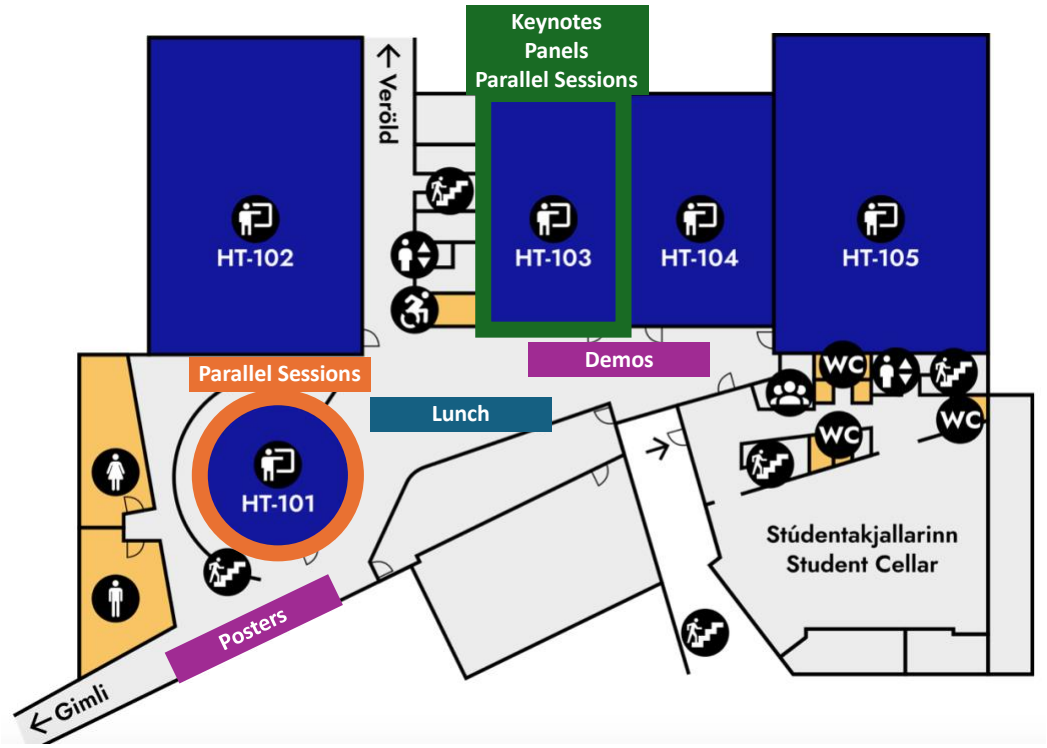

WEDNESDAY TECHNICAL PROGRAM

08:30–09:30	**Keynote 1**
Room HT-103	Chairs: Srividhya Venkataraman, AMD & Younghyun Kim, Purdue University
	Enabling the AI Revolution Michaela Blott, AMD
09:50–11:10	**Session 1A: "Energy Efficient Computing and Storage"**
Room HT-103	Chair: Frank K. Gurkaynak, ETH Zurich
09:50–10:10	***Partial-Sum Quantization Based on Pseudo-Quantization Noise for Variation-Tolerant Analog In-Memory Computing*** **BEST PAPER CANDIDATE** Nameun Kang, EunHyeok Park, Sangsu Park, Jongil Kim, Jaeyun Yi, Jae-Joon Kim
10:10–10:30	***An Analog Multiplier Utilizing an Unconventional Bit-Weighting Scheme with Application to Neural Network Quantization*** Mehdi Kamal, Massoud Pedram
10:30–10:50	***LoRASensE: Learnable Low-Rank Acquisition in Sensors for Efficient Edge Machine Vision*** Yiwen Liang, Zhiqiang Yi, Tianrui Ma, Weidong Cao
10:50–11:10	***AdaGray: An Energy-Efficient Adaptive Gray-Code Strategy for QLC Flash-Memory Storage Systems*** Han-Yu Liao, Jen-Wei Hsieh, Yi-Shen Chen, Chang-Lin Tsai, Yuan-Hao Chang
09:50–11:10	**Session 1B: "Next-Gen EDA: Physical Design Optimization and AI-Driven Methodologies"**
Room HT-101	Chair: Francesco Regazzoni, University of Amsterdam
09:50–10:10	***Simultaneous Optimization of Placement Legalization and Multi-bit Flip-flop Allocation in Physical Design Automation*** Seoyoung Bang, Taewhan Kim
10:10–10:30	***Timing-Driven Macro Placement with Connectivity-Aware Clustering*** Gangmin Jeon, Heechun Park
10:30–10:50	***GenSoC: A Multi-Agent-Assisted SoC Generation Methodology Leveraging Open-Source Hardware*** **BEST PAPER CANDIDATE** Peiran Yan, Qinzhe Zhi, Lifeng Liu, Tianyu Jia
10:50–11:10	***Development of a Physics-Informed Neural Network Model for Rapid Power Integrity Analysis in Die-Level and Die-Package Co-Design for 2.5-D Chiplet Solutions*** Xi Chen, Yuhao Ju, Jie Gu
11:10–12:30	**Special Session 1: "Cold War: Don't Close Your Eyes on Temperature"**
Room HT-103	Chair: Mircea Stan, University of Virginia
11:10–11:30	***Power Map Characterization and Modeling for Commercial CPU/GPUs Considering Temperature Dependence*** Jincong Lu, Sachin Sachdeva, Haotian Lu, Sheldon X.-D. Tan
11:30–11:50	***Thermal Challenges and Opportunities for Off-the-shelf 3D-stacked CPUs*** Jae Yoon Lee, Chae Young Sim, Seung Hun Choi, Sung Woo Chung
11:50–12:10	***Transistor-to-GDS Reliability Analysis in Sub-3nm: Impact of Self-Heating and Aging on Timing*** Swati Deshwal, Hadi Nour Eddine, Mahdi Benkhelifa, Albi Mema, Yogesh S. Chauhan, Hussam Amrouch
12:10–12:30	***Thermal Aware Design Methodologies for System On Chip Application Processor*** Youngsang Cho, Jun So Pak, Seungwook Yoon, Ilryong Kim
11:10–12:30	**Special Session 2: "Neuromorphic Edge Computing: Challenges, Opportunities, and Current Solutions"**
Room HT-101	Chairs: Federico Corradi, Eindhoven University of Technology & Farhad Merchant, University of Groningen
11:10–11:30	***Dynamic Neuromorphic Processing for Energy-Efficient Cognitive Sensing*** Amir Zjajo
11:30–11:50	***Harnessing Sparsity for Low-Power Event-Driven Computing at the Edge*** Orlando Moreira
11:50–12:10	***Reliable and Low-Power Neuromorphic Computing*** Miloš Krstić
12:10–12:30	***Low-Power Neuromorphic Systems: Mixed-Signal Design and Computing-in-Memory for Edge AI*** Farhad Merchant, Federico Corradi
14:00–15:20	**Session 2A: "Brains on a Budget – Smart, Small, and Power-Efficient"**
Room HT-103	Chair: Hussam Amrouch, Technical University of Munich
14:00–14:20	***Exploration of Low-Power Flexible Stress Monitoring Classifiers for Conformal Wearables*** Florentia Afentaki, Sri Sai Rakesh Nakkilla, Konstantinos Balaskas, Paula Carolina Lozano Duarte, Shiyi Jiang, Georgios Zervakis, Farshad Firouzi, Krishnendu Chakrabarty, Mehdi Tahoori
14:20–14:40	***ASAP-FE: Energy-Efficient Feature Extraction Enabling Multi-Channel Keyword Spotting on Edge Processors*** Jongin Choi, Jina Park, Jae-Jin Lee, Massoud Pedram and Woojoo Lee
14:40–15:00	***Minimizing Redundant Checkpoint Triggers for Efficient Intermittent Systems*** **BEST PAPER CANDIDATE** Youngbin Kim, Yoojin Lim

15:00–15:20	***AridWalk: Efficient Graph Random Walks on a Resource-Limited Computational Storage Device*** Liang-Chi Chen, Chien-Chung Ho, Tei-Wei Kuo, Yuan-Hao Chang
14:10–15:20	**Session 2B: "Next-Gen Edge AI: Flash Memory, RISC-V, and Hybrid Architectures"**
Room HT-101	Chair: Thierry Tambe, Stanford University
14:00–14:20	***E-Flash: Energy-Efficient DNN Mapping on NAND Flash Memory with State-Switching Algorithm*** **BEST PAPER CANDIDATE** Gisan Ji, Sanghun Shin, Jangho Baik, Wonbo Shim, Sungju Ryu
14:20–14:40	***Hybrid Systolic Array Accelerator with Optimized Dataflow for Edge Large Language Model Inference*** Chun-Ting Chen, HanGyeol Mun, Jian Meng, Mohamed Abdelfattah and Jae-sun Seo
14:40–15:00	***ID-VSA: Independent and Dynamic Vector Symbolic Architecture for Energy-Efficient Edge AI*** Mehran Shoushtari Moghadam, Abu Kaisar Mohammad Masum, Sercan Aygun, M. Hassan Najafi
15:00–15:20	***RIMIX: RISC-V Core with MIXed-Precision SIMD Instruction Extensions Supported by Oracle-Assisted Sub-Network Search for Efficient TinyML*** Jiyong Park, Dahoon Park, Yeeun Hong, Jaeha Kung
15:50–17:20	**Panel 1 Discussion**
Room HT-103	Organizers and Moderators: Kathy Hoover, AMD & Priyadarshini Panda, Yale University
	Workforce Development in the Era of AI Michaela Blott, AMD Research Chaitali Chakrabarti, ASU Suman Datta, Georgia Tech Sree Menon, Qualcomm Kaushik Roy, Purdue University

THURSDAY TECHNICAL PROGRAM

08:00–09:00	**Keynote 2**
Room HT-103	Chairs: Jerald Yoo, Seoul National University & Srividhya Venkataraman, AMD
	Synthesizable Analog Circuit Design Using Digital Standard Cell Kenichi Okada, Institute of Science Tokyo
09:30–10:50	**Session 3A: "Accelerators for LLM and Edge AI Applications"**
Room HT-103	Chair: M. Hassan Najafi, Case Western Reserve University
09:30–09:50	***Accelerating LLM Inference with Flexible N:M Sparsity via A Fully Digital Compute-in-Memory Accelerator*** BEST PAPER CANDIDATE Akshat Ramachandran, Souvik Kundu, Arnab Raha, Shamik Kundu, Deepak K. Mathaikutty, Tushar Krishna
09:50–10:10	***A Scalable External Memory Access and On-Chip Storage Architecture for Edge-AI Accelerators – Multi-Path Rolling Data Refresh and Layer-Wise Bank Allocation –*** Quan Cheng, Huizi Zhang, Qiufeng Li, Yuan Liang, Mingtao Zhang, Zhenzhe Chen, Ruilin Zhang, Jinjun Xiong, Mingqiang Huang, Longyang Lin, Masanori Hashimoto
10:10–10:30	***FLASH-D: FlashAttention with Hidden Softmax Division*** Kosmas Alexandridis, Vasileios Titopoulos, Giorgos Dimitrakopoulos
10:30–10:50	***A Compact, Low Power Transprecision ALU for Smart Edge Devices*** Ayushi Dube, Gian Singh, Sarma Vrudhula
09:30–10:50	**Session 3B: "Twisting AI and Hardware in 3D"**
Room HT-101	Chair: Bokyung Kim, Rutgers University
09:30–09:50	***MIX-3D: AI-based Architecture-Circuit Co-design Methodology for Mixed-Node, Mixed-Area 3D ICs*** Min Gyu Park, Doyun Kim, Sung Kyu Lim
09:50–10:10	***GAVINA: flexible aggressive undervolting for bit-serial mixed-precision DNN acceleration*** Jordi Fornt, Pau Fontova-Musté, Adrian Gras, Omar Lahyani, Martí Caro, Jaume Abella, Francesc Moll Echeto, Josep Altet
10:10–10:30	***An Open-Source HW-SW Co-Development Framework Enabling Efficient Multi-Accelerator Systems*** Ryan Antonio, Joren Dumoulin, Xiaoling Yi, Josse Van Delm, Yunhao Deng, Guilherme Paim, Marian Verhelst
10:30–10:50	***MemRaptor: Magnetoresistive Array as Matrix Vector Multiplication and Transcendental Function Operator for NLP Applications*** Dong Eun Kim, Tanvi Sharma, Anushka Mukherjee, Mainakh Mukherjee and Kaushik Roy
10:50–12:20	**Tutorial 1: "The Energy Cost of Privacy and Security"**
Room HT-103	Chair: Francesco Regazzoni, University of Amsterdam
	Introduction to Security Primitives and Privacy Preserving Technologies Paolo Palmieri
	Energy Assessment of Security Primitives Ayse Kivilcim Coskun
	Energy Efficient Design and Implementation of Security Primitives Francesco Regazzoni
10:50–12:20	**Tutorial 2: "Autonomy with Neuromorphic System"**
Room HT-101	Chair: Saibal Mukhopadhyay, Georgia Institute of Technology
	Neuromorphic Circuits Amit Trivedi
	Neuromorphic and Hybrid Computing Models Priyadarshini Panda
	Algorithms for Neuromorphic Sensing Systems Saibal Mukhopadhyay
	Neuromorphic Approach to End-to-end Navigation Kaushik Roy
13:50–15:50	**Posters**
1	***On-chip Integrated Voltage Regulators: Frontside, Backside, or Off-Chip?*** Amaan Rahman, Seungmin Woo, Zheng Yang, Sung Kyu Lim
2	***J3DAI: A tiny DNN-Based Edge AI Accelerator for 3D-Stacked CMOS Image Sensor*** Benoit Tain, Raphael Millet, Romain Lemaire, Michal Szczepanski, Laurent Alacoque, Emmanuel Pluchart, Sylvain Choisnet, Rohit Prasad, Jerome Chossat, Pascal Pierunek, Pascal Vivet, Sebastien Thuries
3	***MTA-Coded PAM-4 Receiver with Decision Feedback Power Saving Scheme and Partial DFE for Low-Power Memory Interfaces*** Jusung Lee, Younghwan Chang, Jaekwang Yun, Sanghyuk Seo, Yong-Un Jeong, Suhwan Kim
4	***A High-Performance Dataflow-Based ORB Extractor Accelerator for SLAM*** Rui Xue, Wenming Li, Haibin Wu, Cheng Guo, Yi Li, Xiaochun Ye, Dongrui Fan

5 ***Jack Unit: An Area- and Energy-Efficient Multiply-Accumulate (MAC) Unit Supporting Diverse Data Formats***
Seock-Hwan Noh, Sungju Kim, Seohyun Kim, Daehoon Kim, Jaeha Kung, Yeseong Kim

6 ***Repurpose Accel-Sim for Next Generation NVIDIA Jetson GPU Architectural Design***
Tianhao Huang, Lingyu Sun, Chao Li, Xiaofeng Hou, Yaqian Zhao, Jingwen Leng, Li Li, Minyi Guo

7 ***ML-Power: Machine Learning based Power Estimation for SoCs***
Sujay Pandit, Sujit Dey, Anand Raghunathan

8 ***Diffusion-Enhanced Graph Transformer with Reinforcement Learning for Transferable Analog Circuit Optimizer***
Ho-Jin Lee, Kyeong-Jun Lee, Jaehoon Lee, Kyu-Jin Choi, Geunyong Choi, Youngchang Choi, Kyongsu Lee, Seokhyeong Kang, Jae-Yoon Sim

9 ***SHIFT ECC: A Value Converting HBM ECC Approach for Refresh Energy Efficient Integer Quantized DNN Inference***
Jae Yoon Lee, Young Seo Lee, Young-Ho Gong, Seon Wook Kim, Sung Woo Chung

10 ***Optimizing Heterogeneous Compute-in-Memory with Hybrid Dataflow and In-Network Reduction for Vision Transformer***
Zexin Fu, Yihang Zuo, Yuzhe Ma, Jiayi Huang

11 ***Revisiting Reconfigurable Acceleration of Vision Transformer with Patch Pruning***
Hanning Chen, Yang Ni, Wenjun Huang, Hyunwoo Oh, Tamoghno Das, Fei Wen, Mohsen Imani

12 ***TEE-SFL: Time and Energy-efficient solution for addressing communication heterogeneity in Split Federated Learning Schemes***
Ziyi Zhao, Qifeng Chen, Jingtao Li, Deliang Fan, Chaitali Chakrabarti

13 ***MEbots: Integrating a RISC-V Virtual Platform with a Robotic Simulator for Energy-aware Design***
Giovanni Pollo, Mohamed Amine Hamdi, Matteo Risso, Lorenzo Ruotolo, Pietro Furbatto, Matteo Isoldi, Yukai Chen, Alessio Burrello, Enrico Macii, Massimo Poncino, Daniele Jahier Pagliari, Sara Vinco

14 ***Enhancing Low-Precision Deep Learning: A Posit8 Framework for Energy Efficient DNN Training***
Dongyang Wu, Mehdi Kamal, Massoud Pedram

15 ***Towards Zero-Stall Matrix Multiplication on Energy-Efficient RISC-V Clusters for Machine Learning Acceleration***
Luca Colagrande, Lorenzo Leone, Maximilian Coco, Andrei Deaconeasa, Luca Benini

16 ***Efficient Precision-Scalable Hardware for Microscaling (MX) Processing in Robotics Learning***
Stef Cuyckens, Xiaoling Yi, Nitish Satya Murthy, Chao Fang, Marian Verhelst

17 ***SITRA: Exploiting Temporal Silence in Spiking Transformers for Fast & Energy-efficient Inference***
Abhiroop Bhattacharjee, Abhishek Moitra, Ruokai Yin, Priyadarshini Panda

18 ***DIRC-RAG: Accelerating Edge RAG with Robust High-Density and High-Loading-Bandwidth Digital In-ReRAM Computation***
Kunming Shao, Zhipeng Liao, Jiangnan Yu, Liang Zhao, Qiwei Li, Xijie Huang, Jingyu He, Fengshi Tian, Yi Zou, Xiaomeng WANG, Tim Cheng, Chi Ying Tsui

19 ***upGEMV: A Bandwidth-Efficient and Scalable GEMV Accelerator for PIM Systems***
Fan Yang, Shunchen Shi, Peiheng Zhang, Xueqi Li

20 ***Can Photonic Interconnects be used for High-Throughput Memory Access in FHE Accelerators?***
Dewan Saiham, Mariam Rabadi, Di Wu, Sazadur Rahman

21 ***Sustainably Secure: ChaCha20 Encryption Based on In-Memory Compute***
Samridhi Jain, Mohd Aamir, Anuj Grover

13:50–15:50 **Design Contest Demos**

Chairs: Rajesh Kedia, IITH & Arnab Raha, Intel

1 ***A Sub-10Hz Sub-nW 65nm CMOS Timer with Voltage-Stacking of an Oscillator and Frequency Dividers for Small-Formfactor Scaling-Friendly IoTs***
You Wu, Kei Awano, Hiroaki Kitaike, Kiichi Niitsu

2 ***ECO: Low Power Context-Aware Multimodal AI on NPUs***
Arghadip Das, Yatharth Agarwal, Arnab Raha, Soumendu Ghosh, Vijay Raghunathan

3 ***Radar-PIM-Lite: Ultra-Low-Power PIM Processor for Real-Time UWB Radar Respiration Detection on UAVs***
Kyeongwon Lee, Hyunseok Kwak, Kyeongpil Min, Chaebin Jung, Sangmin Jeon, Woojoo Lee, Jina Park, Massoud Pedram

4 ***A Low-Power Real-Time Hardware Accelerator for Edge Detection Using Stochastic Computing***
Priyajit Ghosh, Rajarshi Mukherjee, Auro Anand Saha, Sutirtha Naha, Arghadip Das, Arnab Raha, Mrinal K Naskar

15:50–17:20 **Panel 2 Discussion**

Room HT-103 Organizer and Moderator: Massoud Pedram, USC

Three Decades of Innovation: The Evolution, Key Contributions, and Future of Low Power Electronics and Design
Jason Cong, UCLA
Giovanni De Micheli, EPFL
Rajiv Joshi, IBM
Hiroshi Nakamura, The University of Tokyo
Kaushik Roy, Purdue University
Mircea Stan, University of Virginia

FRIDAY TECHNICAL PROGRAM

08:00–09:00	**Keynote 3**
Room HT-103	Chairs: Kapil Dev, Nvidia & Younghyun Kim, Purdue University
	From VLSI through Software: Optimizing the Computing Stack for Generative AI Brucek Khailany, Nvidia
09:30–10:50	**Session 4A: "Precision, Performance, and Efficiency: Modern Strategies in ML Systems"**
Room HT-103	Chair: Donghwa Shin, Soongsil University
09:30–09:50	***Faster Ternary and Binary Neural Network Inference on CPU by Reducing Popcount*** **BEST PAPER CANDIDATE** Olivier Fischer, Shien Zhu, Gustavo Alonso
09:50–10:10	***ECLIP: Energy-efficient and Practical Co-Location of ML Inference on Spatially Partitioned GPUs*** Ryan Quach, Yidi Wang, Ali Jahanshahi, Daniel Wong, Hyoseung Kim
10:10–10:30	***SmartMS: Efficient Hierarchical Database Search for Mass Spectrometry*** Flavio Ponzina, Sumukh Pinge, Zheyu Li, Abhijay Deevi, Yilin Ge, Mingu Kang, Tajana Rosing
10:30–10:50	***TruncQuant: Truncation-Ready Quantization for DNNs with Flexible Weight Bit Precision*** Jinhee Kim, Seoyeon Yoon, Taeho Lee, Joo Chan Lee, Kang Eun Jeon, Jong Hwan Ko
09:30–10:50	**Session 4B: "Compute-in-Memory Macros"**
Room HT-101	Chair: Jaehyun Park, University of Ulsan
09:30–09:50	***CAM-CIM: A Hybrid Compute-in-Memory Using Content-Addressable Memory with Subword Split Mapping for Reduced ADC Resolution*** Sangwoo Jung, Hojin Lee, Yejin Lee, Jiyong Park, Dahoon Park, Hyunseob Shin, Jong-Hyeok Yoon, Jaeha Kung
09:50–10:10	***A 20.98TOPS/W Energy-Efficient Binary BERT Model on Group Vector Systolic CIM Accelerator*** Dingbang Liu, Ziyi Guan, Qilong Chen, Jingyun Gu, Jiaqi Yang, Kai Li, Wei Mao, Ngai Wong, Changwen Chen, Hao Yu
10:10–10:30	***Cost-efficient Processing-in-Memory Architecture with Training-free and Universal Error Compensation*** **BEST PAPER CANDIDATE** MyeongJi Yun, Jung Gyu Min, Sein Oh, Jiwoung Choi, Minkyu Je, Jang-Sik Lee, Youngjoo Lee
10:30–10:50	***Design Techniques for Ultra-low Power Cryogenic CMOS for Quantum Computing Applications (Industry)*** Sudipto Chakraborty, Pat Rosno, John Bulzacchelli, David Frank, Rajiv Joshi, Daniel Friedman
10:50–12:10	**Session 5A: "Transceivers and Stochastic Logic Design"**
Room HT-103	Chair: Alexandre Levisse, EPFL
10:50–11:10	***A Spectral-Efficient Low-Power NRZ/PAM-4 Dual-Mode Wireline Transmitter for Multidrop Interfaces*** Donggeon Kim, Kiarash Gharibdoust, Armin Tajalli, Kyungtae Lee, Gain Kim
11:10–11:30	***Energy-Efficient Single-Ended Capacitive PAM-4 Transceiver for Next-Generation HBM Interfaces*** Jaeyoon Kim, Sangyoon Lee, Jaekwang Yun, Sanghyuk Seo, Kwangyeon Lee, Yong-Un Jeong, Suhwan Kim
11:30–11:50	***Always-On Sensing in Energy-Harvested Systems via Stochastic Intermittent Computing*** Sepehr Tabrizchi, Mehran Shoushtari Moghadam, Ali Shafiee Sarvestani, Sercan Aygun, M. Hassan Najafi, Arman Roohi
11:50–12:10	***Design of a correlation-insensitive HFQ stochastic adder by local two-phase clocking*** Yuki Matsumoto, Masamitsu Tanaka, Takatsugu Ono
10:50–12:10	**Session 5B: "Emerging Technologies for Secure and Efficient Computing"**
Room HT-101	Chair: Tianyu Jia, Peking University
10:50–11:10	***DPIMA: A DRAM-Based Processing-in-Memory Accelerator for Privacy-Preserving Machine Learning*** **BEST PAPER CANDIDATE** Bokyung Kim
11:10–11:30	***QuAKE: Speeding up Model Inference Using Quick and Approximate Kernels for Exponential Non-Linearities*** Sai Kiran Narayanaswami, Gopalakrishnan Srinivasan, Ravindran Balaraman
11:30–11:50	***Meta-Heuristic Optimization of Karatsuba Multiplier Designed ECC Processor*** Pruthvi Parate, Daksh Sharma, Alwin Shaju, Vasanthi D R, Madhav Rao
11:50–12:10	***Unicorn-CIM: Unconvering the Vulnerability and Improving the Resilience of High-Precision Compute-in-Memory*** Qiufeng Li, Yiwen Liang, Weidong Cao

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1.1. Technologies and Circuits

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Track 2. CAD, Systems, and Software

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Track 3. Crosscutting Topics

3.1. AI/ML Hardware and Systems

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3.2. Emerging Technologies and Next-Generation Computing

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Sumit Mandal (Track Co-Chair), Indian Institute of Science
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Yuqi Su, Peking University

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Amitabh Das, AMD
Debayan Das, IISC
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Anupam Golder, Intel
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Dirmanto Jap, Nanyang Technological University
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Kaveh Shamsi, University of Texas Dallas
Marc Stöttinger, RheinMain University of Applied Sciences

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Chengwei Zhou

PROGRAM OVERVIEW

103 Room HT-103 101 Room HT-101

Wednesday, Aug. 6	07:00–08:00	Breakfast	
	07:30–08:00	Registration	
	08:00–08:30	**Welcome**	
	08:30–09:30	**Keynote 1** 103 **Michaela Blott, AMD** *"Enabling the AI Revolution"*	
	09:30–09:50	Coffee Break	
	09:50–11:10	**Session 1A** 103 *"Energy Efficient Computing and Storage"*	**Session 1B** 101 *"Next-Gen EDA: Physical Design Optimization and AI-Driven Methodologies"*
	11:10–12:30	**Special Session 1** 103 *"Cold War: Don't Close Your Eyes on Temperature"*	**Special Session 2** 101 *"Neuromorphic Edge Computing: Challenges, Opportunities, and Current Solutions"*
	12:30–14:00	Lunch	
	14:00–15:20	**Session 2A** 103 *"Brains on a Budget – Smart, Small, and Power-Efficient"*	**Session 2B** 101 *"Next-Gen Edge AI: Flash Memory, RISC-V, and Hybrid Architectures"*
	15:20–15:50	Coffee Break	
	15:50–17:20	**Panel 1** 103 **Kathy Hoover, AMD & Priyadarshini Panda, Yale** *"Workforce Development in the Era of AI"*	
Thursday, Aug. 7	07:00–08:00	Breakfast	
	07:30–08:00	Registration	
	08:00–09:00	**Keynote 2** 103 **Kenichi Okada, Institute of Science Tokyo** *"Synthesizable Analog Circuit Design Using Digital Standard Cell"*	
	09:00–09:30	Coffee Break	
	09:30–10:50	**Session 3A** 103 *"Accelerators for LLM and Edge AI Applications"*	**Session 3B** 101 *"Twisting AI and Hardware in 3D"*
	10:50–12:20	**Tutorial 1** 103 *"The Energy Cost of Privacy and Security"*	**Tutorial 2** 101 *"Autonomy with Neuromorphic System"*
	12:20–13:50	Lunch	
	13:50–15:50	**Posters & Design Contest Demos**	
	15:50–17:20	**Panel 2** 103 **Massoud Pedram, USC** "Three Decades of Innovation: The Evolution, Key Contributions, and Future of Low Power Electronics and Design"	
	18:30–21:00	Banquet	
Friday, Aug. 8	07:00–08:00	Breakfast	
	07:30–08:00	Registration	
	08:00–09:00	**Keynote 3** 103 **Brucek Khailany, Nvidia** *"From VLSI through Software: Optimizing the Computing Stack for Generative AI"*	
	09:00–09:30	Coffee Break	
	09:30–10:50	**Session 4A** 103 *"Precision, Performance, and Efficiency: Modern Strategies in ML Systems"*	**Session 4B** 101 *"Compute-in-Memory Macros"*
	10:50–12:10	**Session 5A** 103 *"Transceivers and Stochastic Logic Design"*	**Session 5B** 101 *"Emerging Technologies for Secure and Efficient Computing"*
	12:10–12:40	**Closing Remark and Award Ceremony** 103	
	12:40–14:00	Lunch	