# ISLPED'05

## 2005 International Symposium on Low Power Electronics and Design

**Hotel Marriott del Mar**
**San Diego, California, USA**
**August 8-10, 2005**

*ISLPED 10th Anniversary*

# Message from Chairs

*Welcome to the 10th Anniversary of the International Symposium on Low Power Electronics and Design (ISLPED).*

ISLPED was born in its current form in 1996 through the merger of the International Symposium on Low Power Electronics (ISLPE) and the International Symposium on Low Power Design (ISLPD), each having had two previous editions before the merger. Since its inception, ISLPED has been the premier forum for presentation of advances in all aspects of low power design and technologies, including devices and circuits, logic and micro-architecture, design tools and methodologies, system-level design, and software. The last decade has clearly established power consumption as a primary concern for a wide range of electronic and computing devices, and if left unchecked, power-related issues threaten to de-rail the progress of semiconductor technologies.

This year's 10th anniversary of ISLPED will be marked by an exciting technical program. Industry luminaries Dennis Buss, Vice President of Silicon Technology Development at TI, and Steve Smith, Vice President of the Digital Enterprise Group at Intel, will deliver plenary talks about low power design from an industrial perspective. The conference banquet will feature a panel that re-unites some of the "Founding Fathers" of ISLPED, who started the symposium 10 years ago. The panelists will reminisce about advances in low-power design in the past decade, and will provide their visions of the future for this field and its impact on the semiconductor and electronics industries. Two embedded tutorials will focus on issues in ultra-wideband radio design, and low-power design in FPGAs, while two special sessions will feature invited talks that consider multi-core processing architectures for the power-constrained era, and application drivers such as pervasive and wearable computing.

The technical program includes a rich mixture of academic and industrial papers contributed by researchers from all over the world. The program includes 53 paper presentations and 19 posters, which were selected by the program committee from a record 233 submissions. Five papers have been selected as finalists for a Best Paper Award. The winner of the award will be announced before the end of the conference, based on evaluations of the papers in the proceedings, as well as the presentations made during the conference. The Low-power Design Contest received several original, power-aware designs from universities and research organizations. The best of these submissions will be featured in a special session at the symposium.

ISLPED is sponsored by ACM SIGDA and the IEEE Circuits and Systems Society. It receives technical co-sponsorship from the IEEE Solid State Circuits and the IEEE Electron Devices Societies. The symposium has received generous financial support from Cadence, IBM, Intel, Magma Design Automation, Sequence Design, Synopsys, and Texas Instruments.

We hope that you will find the symposium stimulating and enjoyable.

**Kaushik Roy and Vivek Tiwari**
***General Co-chairs***

**Anand Raghunathan and Mircea Stan**
***Technical Program Co-Chairs***

# ISLPED 2005 Program at a Glance -- Hotel Marriott del Mar

| | Times | Salon A-C | Salon D | Salon E-H |
|---|---|---|---|---|
| Monday, August 8 | 7:30 - 8:30 | | | Breakfast |
| | 8:30 - 8:45 | Opening Welcome | | |
| | 8:45 - 9:45 | Keynote Talk | | |
| | 9:45 - 10:00 | | | Break |
| | 10:00 - 12:00 | Session 1: Technologies and Devices for Low Power | Session 2: Micro-architectural Techniques | |
| | 12:00 - 1:00 | | | Lunch |
| | 1:00 - 3:00 | Session 3: Converter and Communication Circuits | Session 4: (Special Session) Low-power Design for FPGAs | |
| | 3:00 - 4:00 | Poster Session P1: Low-Power Circuit Techniques | Poster Session P2: Logic and Microarchitecture | Poster Interaction & Break |
| | 4:00 - 5:30 | Session 5: Circuit-level Optimizations | Session 6: Special-Purpose Processing | |
| Tuesday, August 9 | 7:45 - 8:45 | | | Breakfast |
| | 8:45 - 9:45 | Plenary Talk | | |
| | 9:45 - 10:00 | | | Break |
| | 10:00 - 12:00 | Session 7: Circuit Techniques for Scaled Technologies | Session 8: Low Power Software Design and Sensing | |
| | 12:00 - 1:00 | | | Lunch |
| | 1:00 - 3:00 | Session 9: Power Grid, Thermal, and Leakage Issues | Session 10: Power Management and Voltage Scaling | |
| | 3:00 - 4:00 | Design Contest Presentations | | Break |
| | 4:00 - 5:30 | Session 11: (Special Session) Hot Topic -- Low-Power Multi-core Architectures | Session 12: (Special Session) Low-power Ultra-Wideband Radios | |
| | 5:45 - 7:30 | | | Banquet and ISLPED 10th Anniversary Panel |
| Wednesday, August 10 | 7:30 - 8:30 | | | Breakfast |
| | 8:30 - 9:30 | Invited Talk | | |
| | 9:30 - 10:30 | Poster Session P3: Power Supply Design | Poster Session P4: I/O and Memory System Design | Poster Interaction & Break |
| | 10:30 - 12:30 | Session 13: Low Power Memory | Session 14: System Design Methodology | |
| | 12:30 | Closing Remarks | | |

# TECHNICAL PROGRAM

## Monday, August 8, 2005

**7:30 – 8:30 Breakfast (Salon E-H)**

**8:30 – 8:45 Opening Welcome (Salon A-D)**
Welcome Message
Vivek Tiwari and Kaushik Roy, General Co-chairs
Symposium Highlights
Anand Raghunathan and Mircea Stan, Program Co-Chairs

**8:45 – 9:45 Keynote Talk:** Technology and Design Challenges for Mobile Communication and Computing Products **(Salon A-D)**
Dennis Buss, Vice President of Silicon Technology Development, Texas Instruments

**9:45 – 10:00 Break (Salon E-H)**

**10:00 – 12:00 Session 1: Technologies and Devices for Low Power (Salon A-C)**
Chair: Chris Kim, Univ. of Minnesota
Co-Chair: Matthew Ziegler, IBM

*1.1* β *FinFET-Based SRAM Design*
Zheng Guo, Sriram Balasubramanian, Radu Zlatanovici, Tsu-Jae King, Borivoje Nikolic
*1.2 Modeling and Analysis of Total Leakage Currents in Nanoscale Double Gate Devices and Circuits*
Saibal Mukhopadhyay, Keunwoo Kim, Ching-Te Chuang, Kaushik Roy
*1.3(s) Effectiveness of Low Power Dual-Vt Designs in Nano-Scale Technologies Under Process Parameter Variations*
Amit Agarwal, Kunhyuk Kang, Swarup K. Bhunia, James D. Gallagher, Kaushik Roy
1.4(s) *Analysis and Mitigation of Variability in Subthreshold Design*
Bo Zhai, Scott McLean Hanson, David Blaauw, Dennis Sylvester
*1.5(s) Measurements and Modeling of Intrinsic Fluctuations in MOSFET Threshold Voltage*
Ali Keshavarzi, Gerhard Schrom, Stephen Tang, Sean Ma, Keith Bowman, Sunit Tyagi, Kevin Zhang, Tom Linton, Nagib Hakim, Steven Duvall, John Brews and Vivek De

**10:00 – 12:00 Session 2: Micro-architectural techniques (Salon D)**
Chair: Marios Papaefthymiou, Univ. of Michigan
Co-chair: Alper Buyuktosunoglu, IBM

*2.1 Instruction Packing: Reducing Power and Delay of the Dynamic Scheduling Logic*
Joseph Sharkey, Dmitry Ponomarev, Kanad Ghose, Oguz Ergin
*2.2 Energy-Efficient and High-Performance Instruction Fetch using a Block-Aware ISA*
Ahmad Zmily, Christos Kozyrakis
*2.3 (s) Energy-Aware Fetch Mechanism: Trace Cache and BTB Customization*
D. Chaver, M. A. Rojas, L. Pinuel, M. Prieto, F. Tirado, M. C. Huang
*2.4 (s) Understanding The Energy Efficiency of SMT and CMP with Multi-clustering.*
Jason Cong, Ashok Jagannathan, Glenn Reinman, Y. Tamir
*2.5 (s) A Simple Mechanism to Adapt Leakage-Control Policies to Temperature*
Stefanos Kaxiras, Polychronis Xekalakis, Georgios Keramidas

**12:00 – 13:00 Lunch (Salon E-H)**

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β Best paper candidate

**13:00 – 15:00 Session 3: Converter and Communication Circuits (Salon A-C)**
Chair: Remus Albu, Philips Research
Co-chair: Gu-Yeon Wei, Harvard Univ.

*3.1* β *A 120nm Low Power Asynchronous ADC*
E. Allier, J. Goulier, G. Sicard, A. Dezzani, E. André, M. Renaudin
*3.2 A 9.5mW 4GHz WCDMA Frequency Synthesizer in 0.13um CMOS*
Xinhua Chen, Qiuting Huang
*3.3(s) A Low Power Current Steering Digital to Analog Converter in 0.18 micron CMOS*
Douglas A. Mercer
3.4*(s) Systematic Power Reduction and Performance Analysis of Mismatch Limited ADC Designs*
Peter C.S. Scholtens, David Smola, Maarten Vertregt
3.5*(s) A Novel Predictive Inductor Multiplier for Integrated Circuit DC-DC Converters in Portable Applications*
L. A. Milner, G. A. Rincón-Mora

**13:00 – 15:00 Session 4 (SPECIAL SESSION): Low-power Design for FPGAs (Salon D)**
Organizer: Lei He, UC Los Angeles
Chair: Chung-Kuan Cheng, UC San Diego

Lei He, UC Los Angeles
Tim Huan, Xilinx
Mike Hutton, Altera
Steve Wilton, Univ. of British Columbia

**15:00 – 16:00 Poster Session P1: Low-power circuit techniques (Presentations: Salon A-C, Interaction: Salon E-H)**
Chair: Steve Kosonocky, IBM

*P1.1 A GHz-Class Charge Recovery Logic*
Visvesh S. Sathe, Marios C. Papaefthymiou, Conrad H. Ziesler
*P1.2 Low-Power Fanout Optimization Using Multiple Threshold Voltage Inverters*
Behnam Amelifard, Farzan Fallah, Massoud Pedram
P1.3 *A Low-Power Bus Design Using Joint Repeater Insertion and Coding*
Srinivasa R. Sridhara, Naresh R. Shanbhag
P1.*4 An 8.3GHz Dual Supply/Threshold Optimized 32b Integer ALU-Register File Loop in 90nm CMOS*
Steven K. Hsu, Amit Agarwal, Kaushik Roy, Ram K. Krishnamurthy, Shekhar Borkar
*P1.5 A Low-Power Multichannel Gated Oscillator-Based CDR for Short-Haul Applications*
Armin Tajalli, Paul Muller, Mojtaba Atarodi, Yusuf Leblebici

**15:00 – 16:00 Poster Session P2: Logic and microarchitecture (Presentations: Salon D, Interaction: Salon E-H)**
Chair: Krste Asanovic, MIT

*P2.1 An Algebraic Decision Diagram (ADD) Based Technique to find Leakage Histograms of Combinational Designs*
Kanupriya Gulati, Nikhil Jayakumar, Sunil P Khatri
*P2.2 Cascaded Carry-Select Adder (C2SA): A New Structure for Low-Power CSA Design*
Yiran Chen, Hai Li, Kaushik Roy, Cheng-Kok Koh
*P2.3 Region-Level Approximate Computation Reuse for Power Reduction in Multimedia Applications*
Xueqi Cheng, Michael S. Hsiao
P2.4 *Joint Exploration of Architectural and Physical Design Spaces with Thermal Consideration*
Yen-Wei Wu, Chia-Lin Yang, Ping-Hung Yu, Y.-W. Chang

β Best paper candidate

P2.5 *Coordinated, Distributed, Formal Energy Management of Chip Multiprocesors*
Philo Juang, Qiang Wu, Li-Shiuan Peh, Margaret Martonosi, D. W. Clark

**16:00 – 17:30 Session 5: Circuit-level optimizations (Salon A-C)**
Chair: Renu Mehra, Synopsys
Co-chair: Barry Pangrle, ArchPro Design Automation

*5.1 β A Probabilistic Framework for Power-Optimal Repeater Insertion in Global Interconnects under Parameter Variations*
V. Wason, K. Banerjee
*5.2(s) Power-optimal Repeater Insertion Considering Vdd and Vth as Design Freedoms*
Yu Ching Chang, King Ho Tam, Lei He
*5.3(s) Probabilistic Dual-Vth Leakage Optimization Under Variability*
Azadeh Davoodi, Ankur Srivastava
5.4(s) *Linear Programming for Sizing, Vth and Vdd Assignment*
David Chinnery, Kurt Keutzer

**16:00 – 17:30 Session 6: Special-purpose processing (Salon D)**
Chair: Dennis Sylvester, Univ. of Michigan
Co-chair: Alice Wang, Texas Instruments

*6.1 β An Efficient Spurious Power Suppression Technique (SPST) and its Applications on MPEG-4 AVC/H.264 Transform Coding Design*
Kuan-Hung Chen, Kuo-Chuan Chao, Jinn-Shyan Wang, Yuan-Sun Chu, Jiun-In Guo
*6.2(s) Cost-Effective Low-Power Processor-In-Memory-based Reconfigurable Datapath for Multimedia Applications*
Marco Lanuzza, Martin Margala, Pasquale Corsonello
*6.3(s) Two Efficient Methods to Reduce Power and Test Time*
Il-Soo Lee, Tony Ambler
6.4(s) *Power and Thermal Effects of SRAM vs. Latch-Mux Design Styles and Clock Gating Choices*
Yingmin Li, M. Hempstead, P. Mauro, David Brooks, Zhigang Hu, Kevin Skadron

## Tuesday, August 9, 2005

**7:45 – 8:45 Breakfast (Salon E-H)**

**8:45 – 9:45 Plenary Talk: Platform Trends for the Digital Home and Enterprise (Salon A-D)**
Steve Smith, Vice President of the Digital Enterprise Group, Intel

**9:45 – 10:00 Break (Salon E-H)**

**10:00 – 12:00 Session 7: Circuit Techniques for Scaled Technologies (Salon A-C)**
Chair: Kevin Yu Cao, Arizona State Univ.
Co-chair: Ali Keshavarzi, Intel
*7.1 Complexity Reduction in an nRERL Microprocessor*
Seokkee Kim, Soo-Ik Chae
*7.2 Driver Pre-emphasis Techniques for On-Chip Global Buses*
Liang Zhang, John Wilson, Rizwan Bashirullah, L. Luo, J. Xu, Paul Franzon
*7.3(s) Multi-Story Power Delivery for Supply Noise Reduction and Low Voltage Operation*
Jie Gu, Chris H. Kim
7.4*(s) Low Power SRAM Techniques for Handheld Products*
Rabiul Islam, Adam Brand, Dave Lippincott
*7.5(s) High Resolution Body Bias Techniques for Reducing the Impacts of Leakage Current and Parasitic Bipolar*
Masaya Sumita

β Best paper candidate

**10:00 – 12:00 Session 8: Low Power Software Design and Sensing (Salon D)**
Chair: Alper Buyuktosunoglu, IBM
Co-Chair: Diana Marculescu, Carnegie Mellon Univ.

*8.1 An Evaluation of Code and Data Optimizations in the Context of Disk Power Reduction*
M. Kandemir, S. W. Son, G. Chen
*8.2 Optimizing Sensor Movement Planning for Energy Efficiency*
Guiling Wang, Mary Jane Irwin, Piotr Berman, Haoying Fu, Tom La Porta
*8.3(s) Power Prediction of Intel Xscale Processors Using Performance Monitoring Unit Events*
Gilberto Contreras, Margaret Martonosi
8.4*(s) Power Reduction by Varying Sampling Rate*
William R. Dieter, Srabosti Datta, Wong Key Kai
8.*5(s) Energy Efficient Strategies for Deployment of a Two-Level Wireless Sensor Network*
Ali Iranli, Morteza Maleki, Massoud Pedram

**12:00 – 13:00 Lunch (Salon E-H)**

**13:00 – 15:00 Session 9: Power grid, thermal, and leakage issues (Salon A-C)**
Chair: Stan Krolikoski, ChipVision

*9.1 Power Grid Voltage Integrity Verification*
Maha Nizam, Farid N. Najm, Anirudh Devgan
*9.2 The Need for a Full-Chip and Package Thermal Model for Thermally Optimized IC Designs*
Wei Huang, Eric B. Humenay, Kevin Skadron, Mircea R. Stan
*9.3(s) Peak Temperature Control and Leakage Reduction During Binding in High Level Synthesis*
Rajarshi Mukherjee, Seda Ogrenci Memik, Gokhan Memik
9.4*(s) LAP: A Logic Activity Packing Methodology for Leakage Power-Tolerant FPGAs*
Hassan Hassan, Mohab Anis, Mohamed Elmasry
9.*5(s) Defocus-Aware Leakage Estimation and Control*
Andrew B. Kahng, Swamy Muddu, Puneet Sharma

**13:00 – 15:00 Session 10: Power Management and Voltage Scaling (Salon D)**
Chair: Sujit Dey, Ortiva Wireless
Co-Chair: Joerg Henkel, Univ. of Karlsruhe

*10.1* $\beta$ *Hierarchical Power Management with Application to Scheduling*
Peng Rong, Massoud Pedram
*10.2 Runtime Identification of Microprocessor Energy Saving Opportunities*
W. Lloyd Bircher, Madhavi Valluri, Jason Law, Lizy K. John
*10.3(s) Energy Efficient SEU-Tolerance in DVS-Enabled Real-Time Systems through Information Redundancy*
A. Ejlali, M.T. Schmitz, B.M. Al-Hashimi, S.G. Miremadi,P. Rosinger
*10.4(s) Bounds on Power Savings Using Runtime Dynamic Voltage Scaling: An Exact Algorithm and A Linear-time Heuristic Approximation*
Fen Xie, Margaret Martonosi, Sharad Malik
10.5(s) *Power Aware Code Scheduling for Clusters of Active Disks*
S. W. Son, G. Chen, M. Kandemir

**15:00 – 16:00 Design Contest Presentations (Salon A-C)**
Chair: David Scott, Texas Instruments

*D1.1 Everlast: Long-life, supercapacitor-operated Wireless Sensor Node*
Farhan Simjee, Pai H. Chou

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$\beta$ Best paper candidate

*D1.2 A Low-Power Embedded SRAM Cache with PVT-Aware Leakage Reduction and Improved Read Stability*
Chris H. Kim, Jae-Joon Kim, Kaushik Roy
*D1.3 Heliomote: Enabling self-sustained wireless sensor networks through solar energy harvesting*
Jason Hsu, Jonathan Friedman, Vijay Raghunathan, Aman Kansal, Mani Srivastava
D1.4 *Low Power State-Parallel Relaxed Adaptive Viterbi Decoder Design and Implementation*
Fei Sun, Tong Zhang
D1.*5 A Low Power Three-Level Differential Encoding for High-Speed Single-Ended Parallel Links*
Sotirios Zogopoulos, Won Namgoong

**16:00 – 17:30 Session 11 (SPECIAL SESSION): Hot Topic – Low-Power Multi-core Architectures (Salon A-C)**
Organizer/Moderator: Trevor Mudge, Univ. of Michigan

Presenters:
Krisztian Flautner, ARM
Kunle Olukotun, Stanford Univ.
Grant Martin, Tensilica

**16:00 – 17:30 Session 12 (SPECIAL SESSION): Low-Power Ultra-Wideband Radios (Salon D)**
Organizer: Payam Heydari, UC Irvine
Chair: Ahmed Eltawil, UC Irvine

Presenters:
Asad Abidi, UC Los Angeles
Payam Heydari, UC Irvine

**17:45 – 19:30 Banquet and ISLPED 10th Anniversary Panel**
Moderator: Andrew B. Kahng, UC San Diego
*Panelists*:
Brock Barton, Texas Instruments
Bob Brodersen, UC Berkeley
Mark Horowitz, Stanford
Massoud Pedram, USC
Jan Rabaey, UC Berkeley

## Wednesday, August 10, 2005

**7:30 – 8:30 Breakfast (Salon E-H)**

**8:30 – 9:30 Invited Talk: Wearable Computing — A Catalyst for Business and Entertainment (Salon A-D)**
Chandra Narayanaswami, Manager, Wearable Computing Group, IBM TJ Watson Research Center

**9:30 – 10:30 Poster Session P3: Power Supply Design (Presentations: Salon A-C, Interaction: Salon E-H)**

Chair: Satyen Mukherjee, Philips

*P3.1 Design and Optimization on Dynamic Power System for Self-Powered Integrated Wireless Sensing Nodes*
Dongsheng Ma, J. M. Wang, Mohankumar N. Somasundaram, Zongqi Hu
*P3.2 Accurate Battery Lifetime Estimation Using High-Frequency Power Profile Emulation*
Farhan Simjee, Pai Chou
P3.3 *On-Chip Digital Power Supply Control for System-on-Chip Applications*
Maurice Meijer, Jose Pineda de Gyvez, Ralph Otten
P3.*4 Self-Timed Circuits for Energy Harvesting AC Power Supplies*
Jeff Siebert, Jamie Collier, Rajeevan Amirtharajah

**9:30 – 10:30 Poster Session P4: I/O and Memory System Design (Presentations: Salon D, Interaction: Salon E-H)**

Chair: Tony Givargis, UC Irvine

*P4.1 A Tunable Bus Encoder for Off-Chip Data Buses*
Dinesh C. Suresh, Banit Agrawal, Walid Najjar
*P4.2 Fast Configurable-Cache Tuning with a Unified Second-Level Cache*
Ann Gordon-Ross, Frank Vahid, Nikil Dutt
*P4.3 Dataflow Analysis for Energy-Efficient Scratch-Pad Memory Management*
Guangyu Chen, Mahmut Kandemir
P4.4 *Energy Reduction in Multiprocessor Systems using Transactional Memory*
Tali Moreshet, R. Iris Bahar, M. Herlihy
P4.*5 Inter-Program Optimizations for Disk Energy Reduction*
Jerry Hom, Ulrich Kremer

**10:30 – 12:30 Session 13: Low Power Memory (Salon A-C)**
Chair: Charles Lefurgy, IBM
Co-chair: Dinesh Somasekhar, Intel

*13.1 PARE: A Power-Aware Hardware Data Prefetching Engine*
Yao Guo, Mahmoud Ben Naser, Csaba Andras Moritz
*13.2 Snug Set-Associative Caches: Reducing Leakage Power while Improving Performance*
Jia-Jhe Li, Yuan-Shin Hwang
*13.3(s) An Energy Efficient TLB Design Methodology*
Dongrui Fan, Zhimin Tang, H. Huang, Guang R. Gao
*13.4(s) Synonymous Address Compaction for Energy Reduction in Data TLB*
Chinnakrishnan S. Ballapuram, Hsien-Hsin S. Lee, Milos Prvulovic
*13.5(s) A Non-Uniform Cache Architecture for Low Power System Design*
Tohru Ishihara, Farzan Fallah

**10:30 – 12:30 Session 14: System Design Methodology (Salon D)**
Chair: Tajana Simunic, Univ. of California, San Diego
Co-chair: Kanishka Lahiri, NEC

*14.1 Replacing Global Wires with an On-Chip Network: A Power Analysis*
Seongmoo Heo, Krste Asanovic
*14.2 A Low-power Crossroad Switch Architecture and Its Core Placement for Network-On-Chip*
Kuei-Chung Chang, Jih-Sheng Shen, Tien-Fu Chen
*14.3(s) System Level Power and Performance Modeling of GALS Point-to-point Communication Interfaces*
Koushik Niyogi, Diana Marculescu
*14.4(s) A Technique for Low Energy Mapping and Routing in Network-on-Chip Architectures*
Krishnan Srinivasan, Karam S. Chatha
*14.5(s) Improving Energy Efficiency by Making DRAM Less Randomly Accessed*
Hai Huang, Kang G. Shin, Charles Lefurgy, Tom Keller

**12:30 Closing Remarks (Salon A-C)**

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