Final Program

ISLPED' 06
INTERNATIONAL SYMPOSIUM ON LOW POWER ELECTRONICS AND DESIGN

http://www.islped.org

Rottach-Egern, Lake Tegernsee (Munich area), Germany
October 4-6, 2006

W E D N E S D A Y (October 4)

8:45-9:00 Opening Welcome (Rm.B)

9:00-9:45 Keynote 1
Session Chair: Wolfgang Nebel (U. of Oldenburg/OFFIS)
Design Challenges for Mobile Communication Devices
Christoph Kutter, Senior VP Products and Systems, Business Group Communication Solutions, Infineon Technologies AG

9:45-10:00 Break (Rms. D, E, F, Riedersteinstüberl, and Upper foyer)

10:00-12:00 Session 1&2
Session 1: Emerging Technologies and Designs for Low Power (Rm.C)
Session Chair: Chris Kim (U. of Minnesota) Co-Chair: Ali Keshavarzi (Intel Corp.)
Analysis of Super Cut-off Transistors for Ultralow Power Digital Logic Circuits (β)
Arijit Raychowdhury, Xunyao Fong, Qikai Chen and Kaushik Roy
Purdue U., La Fayette, IN
Variation-Driven Device Sizing for Minimum Energy Sub-threshold Circuits
Joyce Kwong and Anantha Chandrakasan
Massachussetts Institute of Technology, Cambridge, MA
Robust Level Converter Design for Subthreshold Logic (s)
Ik Joon Chang, Jaejoon Kim and Kaushik Roy
Purdue U., La Fayette, IN and IBM Research, Yorktown, NY
Integrated Solar Energy Harvesting and Storage (s)
Nathaniel Guilar, Albert Chen, T. Kleeburg and R. Armitharajah
U. of California, Davis, CA
Power/Energy Breakdown of Pipelined Nanometer Caches (90nm/65nm/45nm/32nm) (s)
Samuel Rodriguez and Bruce Jacob
U. of Maryland, College Park, MD

Session 2: Microarchitectural Techniques for Low Power (Rm.B)
Session Chair: Russ Joseph (Northwestern U.) Co-Chair: Qing Wu (SUNY Binghamton)
Stall Cycle Redistribution in a Transparent Fetch Pipeline
Eric Hill and Mikko Lipasti
U. of Wisconsin, Madison, WI
Selective Writeback: Exploiting Transient Values for Energy-Efficiency and Performance
Deniz Balkan, Joseph Sharkey, Dimitry Ponomarev and Kanad Ghose
SUNY Binghamton, Binghamton, NY
Energy-Efficient Dynamic Instruction Scheduling Logic through Instruction Grouping (s)
Hiroshi Sasaki, Masaaki Kondo and Hiroshi Nakamura
Tokyo U., Tokyo, Japan
Independent Front-end and Back-end Dynamic Voltage Scaling for a GALS Microarchitecture (s)
Grigorios Magklis, Pedro Chaparro, Jose Gonzalez and Antonio Gonzalez
Intel Labs., Barcelona, Spain
Synergistic Temperature and Energy Management in GALS Processor Architectures (s)
YongKang Zhu and David H. Albonesi
U. of Rochester, Rochester, NY and Cornell U., Ithaca, NY

12:00-13:00 Lunch (Rms. D, E, F, Riedersteinstüberl, and Upper foyer)

13:00-15:00 Session 3&4
Session 3: Circuit Techniques for Scaled Technologies (Rm.C)
Session Chair: Dongsheng Brian Ma (U. of Arizona); Co-chair: Matthew Ziegler (IBM)
A Two-Port SRAM for Real-Time Video Processor Saving 53% of Bitline Power with Majority Logic and Data-Bit Reordering
Hidehiro Fujiwara, Koji Nii, Junichi Miyakoshi, Yuichiro Murachi,Yasuhiro Morita, Hiroshi Kawaguchi and Masahiko Yoshimoto
Kobe U., Kobe, Japan and Kasanawa U., Japan
A High-Speed Variation-Tolerant Interconnect Technique for Sub-threshold Circuits Using Capacitive Boosting
Jonggab Kil, Jie Gu and Chris Kim
U. of Minnesota, Minneapolis, MN
A Dual VDD Boosted Pulsed Bus Technique for Low Power and Low Leakage Operation (s)
Harmander Deogun, Robert Senger, Dennis Sylvester, Richard Brown and Kevin Nowka
U. of Michigan, Ann Arbor, MI, U. of Utah, Salt Lake City, UT and IBM Research, Austin, TX
Time-Borrowing Multi-Cycle On-Chip Interconnects for Delay Variation Tolerance (s)
Keith Bowman, James Tschanz, Muhammad Khellah, Maged Ghoneima, Yehea Ismail and Vivek De
Intel Corp., Portland, OR and Northwestern U., Evanston, IL
A Pulsed Low-Voltage Swing Latch for Reduced Power Dissipation in High-Frequency Microprocessors (s)
Pong-Fei Lu, Nianzheng Cao, Leon Sigal, Pieter Woltgens, R. Robertazzi and D. Heidel
IBM Research, Yorktown, NY

Session 4: Power Management and Application Specific Architectures (Rm.B)
Session Chair: Massoud Pedram (U. of Southern California); Co-chair: Vivek Tiwari (Intel Corp.)
Temporal vision-guided energy minimization for portable displays (β)
Wei-Chung Cheng, Chih-Fu Hsu and Chain-Fu Chao
National Chiao-Tong U., Hsin-Chu, Taiwan
Dynamic Current Modelling at the Instruction Level
Jose A. Rizo-Morente, Miguel Casas-Sanchez and Chris Bleakley
University College, Dublin, Ireland
Reducing Idle Mode Power in Software Defined Radio Terminals (s)
Hyunseok Lee, Chaitali Chakrabati and Trevor Mudge
U. of Michigan, Ann Arbor, MI and Arizona State U., Tempe, AZ
Power Reduction in H.264 Encoder through Algorithmic and Circuits Transformation (s)
Maria Koziri, George Stamoulis and Ioannis Katsavounidis
U. of Thessaly, Volos, Greece and InterVideo, Inc.

Energy-efficient Motion Estimation using Error-Tolerance (s)
Girish Varatkar and Naresh Shanbhag
U.of Illinois, Urbana-Champaign, IL

15:00-16:00 Poster 1 & Industry Session (Coffee break after presentations in Rms. D, E, F, Riedersteinstüberl, and Upper foyer)
Poster Session 1 (Rm.B)
Session Chair: Tanay Karnik (Intel Corp.)
Variability-Aware Device Optimization under ION and Leakage Current Constraints
Javid Jaffari and Mohab Anis
U. of Waterloo, Waterloo, Canada
A 0.5-V FD-SOI Twin-Cell DRAM with Offset-Free Dynamic-VT Sense Amplifiers
Riichiro Takemura, Kiyoo Itoh and Tomonori Sekiguchi
Hitachi, Ltd., Central Research, Tokyo, Japan
Utilizing Reverse Short Channel Effect for Optimal Subthreshold Circuit Design
Tae-Hyoung Kim, Hanyong Eom, John Keane and Chris Kim
U. of Minnesota, Minneapolis, MN
Logic Circuits Operating in Sub-threshold Voltages
Jabulani Nyathi and Brent Bero
Washington State U., Pullman, WA
A New Mismatch-dependent Low Power Technique with Shadow Match-line Voltage-detecting Scheme for CAMs
Jianwei Zhang, Yizheng Ye and Binda Liu
Harbin Inst. of Technology, Harbin, China and Natl. Cheng Kung U., China
Thread-Associative Memory for Multicore and Multithreaded Computing
Shuo Wang and Lei Wang
U. of Connecticut, Storrs, CT
Hierarchical Value Cache Encoding for Off-chip Data Bus
Chung-hsiang Lin and Chia-lin Yang
National Taiwan U., Taipei, Taiwan and IBM STGxSeries Development
Reducing Cache Traffic and Energy with Macro Data Load
Lei Jin and Sangyeun Cho
U. of Pittsburgh, Pittsburgh, PA
Modelling Macromodules for High-Level Dynamic Power Estimation of FPGA-based Digital Designs
Axel Reimer, Arne Schulz and Wolfgang Nebel
U. of Oldenburg and OFFIS, Oldenburg, Germany

Industry Session (Rm.C)
Session Chair: Qing Wu (SUNY Binghamton)
This session is dedicated to showcasing industry highlights of low power products and tools.

16:00-17:30 Session 5&6
Session 5: Thermal and Energy Aware Design (Rm.C)
Session Chair: Domenik Helms (OFFIS); Co-chair: Ulf Schlichtmann (Technical University Munich)
Thermal Via Allocation for 3D ICs Considering Temporally and Spatially Variant Thermal Power
Hao Yu, Yiyu Shi, Lei He and Tanay Karnik
U. of California, Los Angeles, CA and Intel, Hillsboro, OR
Dynamic Thermal Clock Skew Compensation using Tunable Delay Buffers (s)
Ashutosh Chakraborty, Karthik Duraisami, Ashoka Sathanur, Prassanna Sithambaram, Luca Benini, Alberto Macii, Enrico Macii and Massimo Poncino
Politecnico di Torino, Torino, Italy and U. di Bologna, Bologna, Italy
An Efficient Time Slack Allocation Algorithm for Dual-Vdd FPGA Power Reduction (s)
Yan Lin, Yu Hu, Lei He and Vijay Raghunathan
U. of California, Los Angeles, CA and Purdue U., La Fayette, IN
A Novel Approach for Variation Aware Power Minimization during Gate Sizing (s)
V. Mahalingam, N. Ranganathan and Justin E. Harlow III
U. of South Florida, Tampa, FL
Session 6: Energy Management for Sensor and Memory Systems (Rm.B)
Session Chair: Hiroshi Nakamura (U. of Tokyo); Co-chair: Radu Marculescu (Carnegie Mellon U.)
Adaptive Duty Cycling for Energy Harvesting Systems (β)
Jason Hsu, Sadaf Zahedi, Aman Kansal, Mani Srivastava and Vijay Raghunathan
U. of California, Los Angeles, CA and Purdue U., La Fayette, IN
Power Reduction of Multiple Disks Using Dynamic Cache Resizing and Speed Control (s)
Le Cai and Yung-Hsiang Lu
Purdue U., La Fayette, IN
Lifetime Aware Resource Management for Sensor Network Using Distributed Genetic Algorithm (s)
Qinru Qiu, Qing Wu, Daniel Burns and Douglas Holtzhauer
SUNY Binghamton, Binghamton, NY and Air Force Research Lab, Rome, NY
Everlast: Long-life, Supercapacitor-operated Wireless Sensor Node (s)
Farhan Simjee and Pai Chou
U. of California, Irvine, CA

17:30-18:30 Embedded Tutorials 1&2
Embedded Tutorial 1 (Rm.C)
Session Chair: Vivek De (Intel Corp.)
Model to Hardware Matching for nm Scale Technologies
Sani Nassif, IBM Research, Austin, TX

Embedded Tutorial 2 (Rm.B)
Session Chair: Pai Chou (U. of California, Irvine)
Low Power Light-weight Embedded Systems
Majid Sarrafzdeh, F. Dabiri, R. Jafari, T. Massey, A. Nahapetan, University of California, Los Angeles, CA and U. of Texas, Dallas, TX

19:00-21:00 Conference Reception (at hotel "Bachmair am See")
Join colleagues and friends for drinks and a variety of food at hotel "Bachmair am See" and to enjoy the beautiful Bavarian scenery.

T H U R S D A Y (October 5)

9:00-9:45 Keynote 2 (Rm.B)
Session Chair: Mircea Stan (U. of Virginia)
Low Power Design - From Technology Challenge to Great Products
Barry Dennington, CTO, SoC Design Technology NXP Semiconductors

9:45-10:00 Break (Rms. D, E, F, Riedersteinstüberl, and Upper foyer)

10:00-12:00 Session 7&8
Session 7: Leakage Control and Dynamic Power Optimization (Rm.C)
Session Chair: Alberto Macii (Politecnico di Torino); Co-chair: Massimo Poncino (Politecnico di Torino)
A Novel Dynamic Power Cutoff Technique (DPCT) for Active Leakage Reduction in Deep Submicron CMOS Circuits (β)
Baozhen Yu and Michael Bushnell
Rutgers U., New Brunswick, NJ
Analysis and Modeling of Subthreshold Leakage of RT-Components under PTV and State Variation
Domenik Helms, Günter Ehmen and Wolfgang Nebel
U. Oldenburg and OFFIS, Oldenburg, Germany
Power Optimization in a Repeater-Inserted Interconnect Via Geometric Programming (s)
Wing Tai Cheung and Ngai Wong
The U.of Hong Kong, Hong Kong
Input-specific Dynamic Power Optimization for VLSI Circuits (s)
Fei Hu and Vishwani Agrawal
Intel Corp., Folsom, CA and Auburn U., Auburn, AL

Two-phase Fine-grain Sleep Transistor Insertion Technique in Leakage Critical Circuits (s)
Yu Wang, Yongpan Liu, Rong Luo, Huazhong Yang and Hui Wang
Tsinghua U., Beijing, China

Session 8: Memory Hierarchy and Caches (Rm.B)
Session Chair: Bruce Jacob (U. of Maryland); Co-chair: Trevor Mudge (U. of Michigan)
Register File Caching for Energy Efficiency
Hui Zeng and Kanad Ghose
SUNY Binghamton, Binghamton, NY
L-CBF: A Low-Power, Fast Counting Bloom Filter Architecture
Elham Safi, Andreas Moshovos and Andreas Veneris
U. of Toronto, Toronto, Canada
A Low Power SRAM Architecture Based on Segmented Virtual Grounding (s)
Mohammad Sharifkhani and Manoj Sachdev
U. Waterloo, Waterloo, Canada
Process Variation Aware Cache Leakage Management (s)
Ke Meng and Russ Joseph
Northwestern U., Evanston, IL
Substituting Associative Load Queue with Simple Hash Table in Out-of-Order Microprocessors (s)
Alok Garg, Fernando Castro, Michael Huang, Luis Pinuel, Dani Chaver and Manuel Prieto
U. of Rochester, Rochester, NY and U. Complutense Madrid, Spain

12:00-13:00 Lunch (Rms. D, E, F, Riedersteinstüberl, and Upper foyer)

13:00-15:00 Session 9&10
Session 9: RF CMOS Building Blocks (Rm.C)
Session Chair: David Binkley (U. of North Carolina, Charlotte); Co-chair: Domine Leenaerts (Philips)
A Novel Power Optimization Technique for Ultra-low Power RFICs (β)
Amin Shameli and Payam Heydari
U. of California, Irvine, CA
A CMOS Analog Frontend for a Passive UHF RFID Tag
Alessio Facen and Andrea Boni
U. di Parma, Parma, Italy
High-Speed Low-Power Frequency Divider with Intrinsic Phase Rotator
Stephan Henzler and Siegmar Koeppe
Infineon Technologies, Neubiberg, Germany

Session 10: Temperature-aware Design and Microarchitecture (Rm.B)
Session Chair: Peter Feldmann (IBM); Co-chair: Kanishka Lahiri (NEC)
An Optimal Analytical Solution for Processor Speed Control with Thermal Constraints
Ravishankar Rao, Sarma Vrudhula, Chaitali Chakrabarti and Naehyuck Chang
Arizona State U., Tempe, AZ and Seoul National U., Seoul, Korea
Temperature-aware Floorplanning for Microarchitecture Blocks with IPC-Power Dependence Modeling and Transient Analysis
Vidyasagar Nookala, David Lilja and Sachin Sapatnekar
U. of Minnesota, Minneapolis, MN
Power Efficiency for Variation-Tolerant Multicore Processors: A Limits Study (s)
James Donald and Margaret Martonosi
Princeton U., Princeton, NJ
Power-Conscious Configuration Cache Structure and Code Mapping for Coarse-Grained Reconfigurable Architecture (s)
Yoonjin Kim, Ilhyun Park, Kiyoung Choi and Y. Paek
Seoul National U., Seoul, Korea
Dynamic Thermal Management for MPEG-2 Decoding (s)
Wonbok Lee, Kimish Patel and Massoud Pedram
U. of Southern California, Los Angeles, CA

15:00-16:00 Poster Session 2 & Design Contest (Coffee break after presentations in Rms. D, E, F, Riedersteinstüberl, and Upper foyer)

Poster Session 2 (Rm.B)
Session Chair: Qing Wu (SUNY Binghamton)
A Low-Power Active Substrate-Noise Decoupling Circuit with Feedforward Compensation for Mixed-Signal SoCs
Song Guo and Hoi Lee
U. of Texas, Dallas, TX
Power-efficient Pulse Width Modulation DC/DC Converters with Zero Voltage Switching Control
Changbo Long, Sasank Reddy, Sudhakar Pamarti, Lei He and Tanay Karnik
U. of California, Los Angeles, CA and Intel, Hillsboro, OR
Behavioral Modeling of Opamp Gain and Dynamic Effects for Power Optimization of Delta-Sigma Modulators and Pipelined ADCs
Anas A. Hamoui, Tarek Alhajj and Mohammad Taherzadeh-Sani
McGill U., Montreal, Canada
Low-power Fanout Optimization by Using MTCMOS and Multi-Vth Techniques
Behnam Amelifard, Farzan Fallah and Massoud Pedram
U.of Southern California, Los Angeles, CA and Fujitsu Labs., CA
A New Strategy for Jointly Optimizing Gate Sizing and Supply Voltage in Ultra-Low Energy Circuits
Scott Hanson, Dennis Sylvester and David Blaauw
U. of Michigan, Ann Arbor, MI
Considering Process Variations During System-Level Power Analysis
Saumya Chandra, Kanishka Lahiri, Anand Raghunathan and Sujit Dey
U. of California, San Diego, CA and NEC Labs, Princeton, NJ
Synchronization-Driven Dynamic Speed Scaling for MPSoCs
Mirko Loghi, Massimo Poncino and Luca Benini
Politecnico di Torino, Italy and U. di Bologna, Italy
Power Phase Availability in a Commercial Server Workload
Lloyd Bircher and Lizy John
U. of Texas, Austin, TX
Reducing Power through Compiler-Directed Barrier Synchronization Elimination
Mahmut Kandemir and Seung Woo Son
Penn State U., University Park, PA
Minimizing Energy Consumption of Banked Memories Using Data Recomputation
Hakduran Koc, Ozcan Ozturk, Mahmut Kandemir, Sri H. K. Narayanan and Ehat Ercanli
Syracuse U., Syracuse, NY and Penn State U., University Park, PA

Design Contest Session (Rm.C)
Session Chair: Barry Pangrle (Atrenta)
This session will include presentations from the winners of the Low Power Design Contest.

16:00-17:00 Embedded Tutorials 3&4
Embedded Tutorial 3 (Rm.C)
Session Chair: Sachin Sapatnekar (U. of Minnesota)
Achieving Femto-Joule Operation: Practical Studies in the Development of Subthreshold Design Techniques
S. Hanson, B. Zhai, David Blaauw, Dennis Sylvester, A. Bryant, X. Wang, University of Michigan, Ann Arbor, MI and IBM Research, Yorktown, NY
Sub-Threshold Design: The Challenges of Minimizing Circuit Energy
B. H. Calhoun, A. Wang, N. Verma, A. Chandrakasan
U. of Virginia, Charlottsville, VA, Massachusetts Institute of Technology, Cambridge, MA and Texas Instruments, TX

Embedded Tutorial 4 (Rm.B)
Session Chair: Philippe Royannez (Texas Instruments)
Design and Power Management of Energy Harvesting Embedded Systems
Vijay Raghunathan, NEC Labs, Princeton, NJ and Pai Chou, U. of California, Irvine, CA

17:30-22:00 Social Event
Attendees will travel up the Wallberg mountain to a mountaintop restaurant for an evening filled with beautiful views and tasty food (and Bavarian beer,

of course). Transportation is provided via gondolas, enterprising participants can also consider hiking up the mountain.

F R I D A Y (October 6)

9:00-9:45 Best Paper Announcement and Panel (Rm.B)
Panel: Flexibility and Low Power; a Contradiction in Terms? - Can Configurable or Re-Configurable Computing Offer Solutions?
Moderator: Peter Wintermayr, Editor in Chief Markt und Technik
Panelists: Reiner Hartenstein, Univ. Kaiserslautern
Heinrich Meyr, RWTH Aachen University and Chief Scientific Officer CoWare, San Jose, US
Steve Leibson, Tensilica

9:45-10:00 Break (Rms. D, E, F, Riedersteinstüberl, and Upper foyer)

10:00-12:00 Session 11&12
Session 11: Low Power, Low Voltage Circuits and DC/DC Converters (Rm.C)
Session Chair: Ben Calhoun (U. of Virginia); Co-chair: Seonghwan Cho (KAIST)
Efficient Scan-Based BIST Scheme for Low Power Dissipation during testing of VLSI chips (s)
Malav Shah
Inst. of Information & Communication Technology, Gujarat, India
Modeling and Analysis of Leakage Induced Damping Effect in Low Voltage LSIs (s)
Jie Gu, John Keane and Chris Kim
U. of Minnesota, Minneapolis, MN
Dithering Skip Modulator with a Novel Load Sensor for Ultra-wide-load High-Efficiency DC-DC Converters (s)
Hong-Wei Huang, Hsin-Hsin Ho, Ke-Horng Chen and Sy-Yen Kuo
National Taiwai U., Taipei, Taiwan
Adaptive On-Chip Power Supply with Robust One-Cycle Control Technique (s)
Dongsheng Ma, J. Wang and Pablo Vazquas
U. of Arizona, Tucson, AZ
Robust Multiple-Phase Switched-Capacitor DC-DC Converter with Digital Interleaving Regulation Scheme (s)
Dongsheng Ma
U. of Arizona, Tucson, AZ

Session 12: Low Power Architectures and Systems (Rm.B)
Session Chair: Yung-Hsiang Lu (Purdue U.); Co-chair: Vijay Raghunathan (NEC)
A Low Power Viterbi Decoder Implementation Using Scarce State Transition and Path Pruning Scheme for High Throughput Wireless Applications
Jie Jin and Chi-ying Tsui
HKUST, Hong Kong
SmartSaver: Turning Flash Drive into a Disk Energy Saver for Mobile Computers
Feng Chen, Song Jiang and Xiaodong Zhang
Ohio State U., Columbus, OH
An Energy-Efficient Virtual Memory System with Flash Memory as the Secondary Storage (s)
Hung-Wei Tseng, Han-Lin Li and Chia-Lin Yang
National Taiwan U., Taipei, Taiwan
Maximizing the Lifetime of Embedded Systems Powered by Fuel Cell-Battery Hybrids (s)
Jianli Zhuo, Chaitali Chakrabarti, Naehyuck Chang and Sarma Vrudhula
Arizona State U., Tempe, AZ and Seoul National U., Seoul, Korea

12:00-12:10 Wrap-up

12:10-13:00 Lunch (only tutorial participants) (Riedersteinstüberl)

13:00-16:00 Half-Day Tutorial (Rm.D)
Leakage Currents in Nanometer CMOS
Domenik Helms, Wolfgang Nebel, OFFIS
Ali Keshavarzi, Intel Corp.

**(s) denotes Short Presentation*
**(β) denotes Best Paper Award Nominee*

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