International Symposium on Low Power Electronics and Design

August 11-13, 2008

National Science Seminar Complex, Indian Institute of Science
Bangalore, India

Sponsored By

with Technical Support From

ISLPED 2008 Platinum Corporate Supporter

ISLPED 2008 Gold Corporate Supporters

ISLPED 2008 Silver Corporate Supporters

ISLPED 2008 Bronze Corporate Supporter

ISLPED 2008 Academic Supporters

Indian Institute of Science

ISLPED 2008 Program

Monday August 11, 2008

08:30-08:45	***Welcome by General and Program Co-Chairs***	
08:45-09:45	***Towards a Green Electronic World: A Collaborative Approach*** Jaswinder Ahuja (Cadence Design Systems, Inc.) [J.N. Tata Auditorium]	
09:45-10:00	*Break*	
10:00-12:00	**Hall A**	**Hall B**
	Session 1.1.2: Variation Tolerant Circuits Session Chair: Niraj Bindal (Intel) Session Co-Chair: Chris Kim (University of Minnesota)	**Session 2.1.1: Power Optimization** Session Chair: Wolfgang Nebel (University of Oldenburg) Session Co-Chair: Nagarajan Ranganathan (University of South Florida)
	Correlation Verification between Transistor Variability Model with Body Biasing and Ring Oscillation Frequency in 90nm Subthreshold Circuits Hiroshi Fuketa, Masanori Hashimoto, Yukio Mitsuyama, Takao Onoye (Osaka University and JST, CREST)	*Dynamic Virtual Ground Voltage Estimation for Power Gating* Hao Xu, Ranga Vemuri, Wen-Ben Jone (University of Cincinnati)
	Optimal Technology Selection for Minimizing Energy and Variability in Low Voltage Applications Mingoo Seok, Dennis Sylvester, David Blaauw (University of Michigan)	*A Mathematical Solution to Power Optimal Pipeline Design by Utilizing Soft Edge Flip-Flops* Mohammad Ghasemazar, Behnam Amelifard, Massoud Pedram (University of Southern California)
	Post-Silicon Programmed Body-Biasing Platform Suppressing Device Variability in 45 nm CMOS Technology Hiroaki Suzuki, Masanori Kurimoto, Tadao Yamanaka, Hidehiro Takata (Renesas Technology Corp.), Hiroshi Makino (Osaka Institute of Technology), Hirofumi Shinohara (Renesas Technology Corp.)	*(S) Power-Gating-Aware High-Level Synthesis* Eunjoo Choi (LG Electronics), Changsik Shin (KAIST), Taewhan Kim (Seoul National University), Youngsoo Shin (KAIST)
	Enhancing Beneficial Jitter Using Phase-Shifted Clock Distribution Dong Jiao, Jie Gu, Pulkit Jain, Chris Kim (University of Minnesota)	*(S) A Parallel and Randomized Algorithm for Large-Scale Discrete Dual-Vt Assignment and Continuous Gate Sizing* Tai-Hsuan Wu, Lin Xie, Azadeh Davoodi (University of Wisconsin)
		(S) Multiple Power-Gating Domain (Multi-VGND) Architecture For Improved Leakage Power Reduction Ashoka Sathanur (Politecnico di Torino), Luca Benini (Università di Bologna), Alberto Macii, Enrico Macii, Massimo Poncino (Politecnico di Torino)
12:00-13:00	*Lunch*	
13:00-15:00	**Hall A**	**Hall B**
	Session 1.1.3: Power Delivery and Timing Session Chair: Swarup Bhunia (Case Western RU) Session Co-Chair: Radu Zlatanovici (Cadence Berkeley Labs)	**Session 2.1.2: Variability-Aware Optimization** Session Chair: Bharadwaj Amrutur (IISC) Session Co-Chair: Vishwani Agarwal (Auburn University)
	A Multi-Story Power Delivery Technique for 3D Integrated Circuits Pulkit Jain, Tae-Hyoung Kim, John Keane, Chris H. Kim (University of Minnesota)	*An Expected-Utility Based Approach to Variation Aware VLSI Optimization Under Scarce Information* Upavan Gupta, Nagarajan Ranganathan (University of South Florida)
	Energy Harvesting Photodiodes with Integrated 2D Diffractive Storage Capacitance Nathaniel J. Guilar, Erin G. Fong, Travis Kleeburg, Diego R.. Yankelevich, Rajeevan Amirtharajah (University of California, Davis)	*SRAM Methodology for Yield and Power Efficiency: Per-Element Selectable Supplies and Memory Reconfiguration Schemes* Rouwaida Kanj (IBM Austin Research Laboratories), Rajiv V. Joshi (IBM T.J. Watson Laboratories), Zhou Li, JB Kuang, Hung Ngo (IBM Austin Research Laboratories), Ying Zhou, Weiping Shi (Texas A&M University), Sani Nassif (IBM Austin Research Laboratories)
	Reducing Wakeup Latency and Energy of MTCMOS Circuits via Keeper Insertion Charbel J. Akl, Magdy A. Bayoumi (University of Louisiana at Lafayette)	*(S) Row/Column Redundancy to Reduce SRAM Leakage in Presence of Random Within-Die Delay Variation* Maziar Goudarzi, Tohru Ishihara (Kyushu University)
	Low-Power High-Accuracy Timing Systems for Efficient Duty Cycling Thomas Schmid, Jonathan Friedman, Zainul Charbiwala, Young H. Cho, Mani B. Srivastava (University of California, Los Angeles)	*(S) Reliability-centric Gate Sizing with Simultaneous Optimization of Soft Error Rate, Delay and Power* Koustav Bhattacharya, Nagarajan Ranganathan (University of South Florida)

		(S) Variation-Aware Gate Sizing and Clustering for Post-Silicon Optimized Circuits Cheng Zhuo, David Blaauw, Dennis Sylvester (University of Michigan)	
15:00-15:15	*Break*		
15:15-17:15	**Hall A**	**Hall B**	**J.N. Tata Auditorium**
	Tutorial: *Low Power Design under Parameter Variations* Swarup Bhunia (Case Western Reserve University), Kaushik Roy (Purdue University)	**Session 1.1.1: Low Voltage Logic and Memory** Session Chair: Hiroaki Suzuki (Renesas) Session Co-Chair: Matt Ziegler (IBM)	**Tutorial:** *Power Management Solutions for Computer Systems and Datacenters* Karthick Rajamani, Charles Lefurgy, Soraya Ghiasi, Juan Rubio, Heather Hanson, Tom Keller (IBM Austin Research Laboratories)
		Error-Resilient Low-Power Viterbi Decoders Rami A. Abdallah, Naresh R. Shanbhag (University of Illinois at Urbana Champaign)	
		Increasing Minimum Operating Voltage (VDDmin) with Number of CMOS Logic Gates and Experimental Verification with up to 1Mega-Stage Ring Oscillators Taro Niiyama, Zhe Piao, Koichi Ishida (University of Tokyo), Masami Murakata (STARC), Makoto Takamiya, Takayasu Sakurai (University of Tokyo)	
		Thermal Analysis of 8-T SRAM for Nano-Scaled Technologies Mesut Meterelliyoz, Jaydeep P. Kulkarni, Kaushik Roy (Purdue University)	
		Analyzing Static and Dynamic Write Margin for Nanometer SRAMs Jiajing Wang, Satyanand Nalam, Benton H. Calhoun (University of Virginia)	
17:15-18:45	**Panel:*Penalty For Power Reduction - Performance or Schedule or Yield?*** Bodhisatya Sarker (Cadence Design Systems (I) Pvt Ltd) Nicco Bhabu (Cadence Design Systems (I) Pvt Ltd) Arijit Dutta (Freescale Semiconductors) Srinath D. (Kawasaki Micro) Kaip Sridhar (Marvel Technologies) Radhakrishnan Nair (SanDisk India) Jayant Lahiri (ARM India) [J.N. Tata Auditorium]		
	Tuesday August 12, 2008		
08:30-10:00	**Hall A**	**Hall B**	
	Session 2.3.1: Adaptive Algorithms for Energy-efficient Applications Session Chair: Chi-Ying Tsui (Hong Kong University of Science and Technology) Session Co-Chair: Karthick Rajamani (IBM Austin Research Laboratories)	**Session 2.2.2: Multi-core Power Optimization** Session Chair: Mary Jane Irwin (Penn State University) Session Co-Chair: Joerg Henkel (University of Karlsruhe)	
	Caching for Bursts (C-Burst): Let Hard Disks Sleep Well and Work Energetically Feng Chen, Xiaodong Zhang (The Ohio State University)	*Proactive Temperature Management in MPSoCs* Ayse Kivilcim Coskun, Tajana Simunic Rosing (University of California, San Diego), Kenny C. Gross (Sun Microsystems)	
	(S) 3-Tier Dynamically Adaptive Power-Aware Motion Estimator for H.264/AVC Video Encoding Muhammad Shafique, Lars Bauer, Jörg Henkel (University of Karlsruhe)	*Entry Control in Network-on-Chip for Memory Power Reduction* Dongwook Lee (Seoul National University), Sungjoo Yoo (POSTECH), Kiyoung Choi (Seoul National University)	
	(S) Energy Conservation by Adaptive Feature Loading for Mobile Content-Based Image Retrieval Karthik Kumar, Yamini Nimmagadda, Yu-Ju Hong, Yung-Hsiang Lu (Purdue University)	*PowerAntz: Distributed Power Sharing Strategy for Network on Chip* Suman K. Mandal, Rabi N. Mahapatra (Texas A&M University)	
	(S) Extending the Lifetime of Media Recorders Constrained by Battery and Flash Memory Size Younghyun Kim, Youngjin Cho, Naehyuck Chang (Seoul National University), Chaitali Chakrabarti (Arizona State University), Nam Ik Cho (Seoul National University)		
10:00-10:15	*Break*		
10:15-11:15	***System Implications of Integrated Photonics*** Norman P. Jouppi (Hewlett-Packard Laboratories) [J.N. Tata Auditorium]		
11:15-12:15	**Hall A**	**Hall B**	
	Poster Session	**Design Contest Session**	

	Design of Dual Threshold Voltages Asynchronous Circuits Behnam Ghavami, Hossein Pedram (Amirkabir University of Technology)	*A low-power CMOS code-modulated multi-purpose dual-antenna receiver front-end* F. Tzeng, A. Jahanian, D. Pi, P. Heydari (University of California, Irvine)	
	O2C: Occasional Two-Cycle Operations for Dynamic Thermal Management in High Performance In-Order Microprocessors Swaroop Ghosh, Jung-Hwan Choi, Patrick Ndai, Kaushik Roy (Purdue University)	*A 150mV, process variation tolerant Schmitt trigger based sub-threshold SRAM* J. P. Kulkarni, K. Roy (Purdue University)	
	Low Power High Bandwidth Amplifier with RC Miller and Gain Enhanced Feedforward Compensation Shagun Bajoria, Vineet Kumar Singh, Raju Kunde, Chetan D. Parikh (Dhirubhai Ambani Institute of Information and Communication Technology)	*Energy metering for free: augmenting switching regulators for real-time monitoring* P. Dutta (UC Berkeley), M. Feldmeier (MIT), J. Taneja (UC Berkeley), J. Paradiso (MIT), D. Culler (UC Berkeley)	
	Single Stage Static Level Shifter Design for Subthreshold to I/O Voltage Conversion Yi-Shiang Lin, Dennis M. Sylvester (University of Michigan)		
	Power Reduction in On-Chip Interconnection Network by Serialization Madan Arvind, Bharadwaj Amrutur (Indian Institute of Science)		
	A Probabilistic Technique for Full-chip Leakage Estimation Shaobo Liu , Qinru Qiu, Qing Wu (Binghamton University, State University of New York)		
	Bus Encoding for Simultaneous Delay and Energy Optimization Jingyi Zhang, Qing Wu, Qinru Qiu (Binghamton University, State University of New York)		
	Frequency Planning for Multi-Core Processors Under Thermal Constraints Michael Kadin, Sherief Reda (Brown University)		
	Reducing Leakage Power by Accounting for Temperature Inversion Dependence in Dual-Vt Synthesized Circuits Andrea Calimera (Politecnico di Torino), R. Iris Bahar (Brown University), Enrico Macii, Massimo Poncino (Politecnico di Torino)		
	Variability of Flip-Flop Timing at Sub-Threshold Voltages Niklas Lotze, Maurits Ortmanns, Yiannos Manoli (University of Freiburg)		
	Low Power Current Mode Receiver With Inductive Input Impedance Marshnil V. Dave, Maryam Shojaei Baghini, Dinesh Sharma (Indian Institute of Technology, Bombay)		
	Analytical Results for Design Space Exploration of Multi-core Processors Employing Thread Migration Ravishankar Rao, Sarma Vrudhula, Krzysztof Berezowski (Arizona State University)		
	A Physical Level Study and Optimization of CAM-Based Checkpointed Register Alias Table Elham Safi, Andreas Moshovos, Andreas Veneris (University of Toronto)		
12:15-13:15	*Lunch*		
13:15-14:15	**Hall A**	**Hall B**	**J.N. Tata Auditorium**
	Session 1.2.1: Memory Systems & Special-purpose Hardware Session Chair: Vasantha Erraguntla (Intel) Session Co-Chair: Alper Buyuktosunoglu (IBM)	**Session 1.3.1: Low-Power Challenges in Analog and Mixed-Signal Front-ends** Session Chair: Kameran Azadet (LSI) Session Co-Chair: William Li (Intel)	**Tutorials**
	Enhancing Energy Efficiency of Processor-Based Embedded Systems through Post-Fabrication ISA Extension Hamid Noori (Institute of Systems, Information Technologies and Nanotechnologies), Farhad Mehdipour, Koji Inoue, Kazuaki Murakami (Kyushu University)	*Optimal Power and Noise Allocation for Analog and Digital Sections of a Low Power Radio Receiver* Kannan Aryaperumal Sankaragomathi, Manodipan Sahoo, Satyam Dwivedi, Bharadwaj S. Amrutur, Navakanta Bhat (Indian Institute of Science)	**Tutorial:** *A Tutorial on Test Power* Vishwani D. Agrawal (Auburn University)

	Energy-Efficient MESI Cache Coherence with Pro-Active Snoop Filtering for Multicore Microprocessors Avadh Patel, Kanad Ghose (State University of New York Binghampton)	*Design of Low-Power Short-Distance Opto-Electronic Transceiver Front-Ends with Scalable Supply Voltages and Frequencies* Xuning Chen (Princeton University), Gu-Yeon Wei (Harvard University), Li-Shiuan Peh (Princeton University)	
14:15-15:15	*(S) A Low Power Layered Decoding Architecture for LDPC Decoder Implementation for IEEE 802.11n LDPC Codes* Jie Jin, Chi-Ying Tsui (The Hong Kong University of Science and Technology)	*(S) On the Power Efficiency of Cascode Compensation over Miller Compensation in Two-Stage Operational Amplifiers* Hamed Aminzadeh, Khalil Mafinezhad (Ferdowsi University of Mashhad)	**Tutorial:** *Power Delivery for High Performance Microprocessors* Srikanth Balasubramanian (Intel Corporation)
	(S) A Secure and Low-Energy Logic Style Using Charge Recovery Approach Mehrdad Khatir, Amir Moradi, Alireza Ejlali, Mohammad T. Manzuri Shalmani, Mahmoud Salmasizadeh (Sharif University of Technology)	*(S) A 1-V Piecewise Curvature-corrected CMOS Bandgap Reference* Jing-hu Li, Yu-nan Fu, Yong-sheng Wang (Harbin Institute of Technology)	
	(S) Word-Interleaved Cache: An Energy Efficient Data Cache Architecture T. Venkata Kalyan, Madhu Mutyam (Indian Institute of Technology Madras)	*(S) A 1.8/2.4-GHz Dual-band CMOS Low Noise Amplifier Using Miller Capacitance Tuning* Deepak Balemarthy, Roy Paily (Indian Institute of Technology, Guwahati)	
15:15-15:30	*Break*		
15:30-16:30	***Innovations to Extend CMOS Nano-transistors to the Limit*** Tahir Ghani (Intel Corporation) [J.N. Tata Auditorium]		
16:30-18:00	**Panel:** ***Power Management from Cores to Datacenters: Where are we going to get the next ten-fold improvements?*** Parthasarathy Ranganathan (Hewlett Packard Labs) [J.N. Tata Auditorium]		
19:00	***Banquet: Classical Indian Dance*** [Atria Hotel]		
	Wednesday August 13, 2008		
08:00-09:30	**Hall A**	**Hall B**	
	Industry Session	**Session 2.2.3: Run-time Power & Thermal Management** Session Chair: Rabi N. Mahapatra (Texas A&M University) Session Co-Chair: Massimo Poncino (Politecnico di Torino)	
	SOC Designs in the Energy Conscious Era Srikanth Jadcherla (Synopsys Inc.)	*Simultaneous Optimization of Battery-Aware Voltage Regulator Scheduling with Dynamic Voltage and Frequency Scaling* Youngjin Cho, Younghyun Kim, Yongsoo Joo, Kyungsoo Lee, Naehyuck Chang (Seoul National University)	
	Tutorial: *Clock Gating for Power Optimization in ASIC Design Cycle : Theory & Practice* Jairam S, Madhusudan Rao, Jithendra Srinivas, Parimala Vishwanath, Udayakumar H., Jagdish Rao (Texas Instruments)	*Expected System Energy Consumption Minimization in Leakage-Aware DVS Systems* Jian-Jia Chen, Lothar Thiele (Swiss Federal Institute of Technology (ETH) Zurich)	
		Hybrid Dynamic Thermal Management Based on Statistical Characteristics of Multimedia Applications Inchoon Yeo, Eun Jung Kim (Texas A&M University)	
09:30-09:45	*Break*		
09:45-10:45	***Advances in Low Power Verification*** Janick Bergeron (Synopsys, Inc.) [J.N. Tata Auditorium]		
10:45-12:15	**Hall A**	**Hall B**	
	Tutorial: *Low Power Chips: A Fabless ASIC Perspective* Shashank Bhonge (Open-Silicon Research Pvt. Ltd), Vamsi Boppana (Open-Silicon, Inc.)	**Session 2.2.1: System-Level Power Estimation** Session Chair: Todd Austin (University of Michigan) Session Co-Chair: Naehyuck Chang (Seoul National University)	
		A Framework for Energy Consumption Based Design Space Exploration for Wireless Sensor Nodes Sonali Chouhan, M. Balakrishnan, Ranjan Bose (Indian Institute of Technology Delhi)	
		Full-System Chip Multiprocessor Power Evaluations Using FPGA-Based Emulation Abhishek Bhattacharjee, Gilberto Contreras, Margaret Martonosi (Princeton University)	
		Noninvasive Leakage Power Tomography of Integrated Circuits by Compressive Sensing Davood Shamsi, Petros Boufounos, Farinaz Koushanfar (Rice University)	

12:15-13:15	*Lunch*		
13:15-15:15	**Hall A**	**Hall B**	
	Tutorial: *On Leakage Currents: Sources and Reduction for Transistors, Gates, Memories and Digital Systems* Wolfgang Nebel (University of Oldenburg), Domenik Helms (OFFIS Research Institute)	**Session 1.2.2: Microarchitectural Techniques** Session Chair: Masaaki Kondo (University of Tokyo) Session Co-Chair: Koji Inoue (Kyushu University)	
		Impact of Dynamic Voltage and Frequency Scaling on the Architectural Vulnerability of GALS Architectures Niranjan Soundararajan, Vijaykrishnan Narayanan, Anand Sivasubramaniam (The Pennsylvania State University)	
		Instruction-Driven Clock Scheduling with Glitch Mitigation Gu-Yeon Wei, David Brooks, Ali Durlov Khan, Xiaoyao Liang (Harvard University)	
		(S) Thread Fusion José González, Qiong Cai, Pedro Chaparro, Grigorios Magklis (UPC-Intel Lab Barcelona), Ryan Rakvic (United States Naval Academy, Annapolis), Antonio González (UPC-Intel Lab Barcelona)	
		(S) Power-Efficient Clustering via Incomplete Bypassing Eric P. Villasenor, DaeHo Seo, Mithuna S. Thottethodi (Purdue University)	
		(S) Lazy Instruction Scheduling: Keeping Performance, Reducing Power Ali Mahjur (Shahid Beheshti University), Mahmud Taghizadeh, Amir Hossein Jahangir (Sharif University of Technology)	
15:15-15:30	*Break*		
15:30-16:30	***On the Rules of Low-Power Design (and How to Break Them)*** Todd M. Austin (University of Michigan) [J.N. Tata Auditorium]		
16:30-17:30	***Next-Generation Power-Aware Design*** Takayasu Sakurai (The University of Tokyo) [J.N. Tata Auditorium]		
17:30	***Closing Remarks*** [J.N. Tata Auditorium]		